International Journal on
"Technical and Physical Problems of Engineering"
(IJTPE)
Published by International Organization of IOTPE

ISSN 2077-3528
IJTPE Journal
www.iotpe.com
ijtpe@iotpe.com

March 2015 | Issue 22 | Volume 7 | Number 1 | Pages 58-64

INVESTIGATING PULSE WIDTH MODULATION METHODS IN MULTILEVEL INVERTERS AND PROPOSITION OF A NOVEL METHOD FOR 27-LEVEL HYBRID INVERTERS

A.R. Pirouznia [1] H. Hatami [1] N.M. Tabatabaei [1,2] A. Jafari [1]

1. Electrical Engineering Department, Seraj Higher Education Institute, Tabriz, Iran
alirezapirouznia@ymail.com, hojat_hatamie@yahoo.com, n.m.tabatabaei@gmail.com, ali.jafari.860@gmail.com
2. Taba Elm International Institute, Tabriz, Iran

Abstract- In recent years, the use of multilevel inverters due to their many advantages such as high harmonic quality has been increased significantly. The present article reviews the structure and operation of two types of such inverters called Neutral Point Diode Clamped and hybrid inverters along with the description of switching methods of each inverter based on pulse width modulation concept. Through comparing the results from harmonic quality view, advantages and disadvantages of each of these transducers with respect to each other and themselves in various switching conditions are discovered. Then a new method for controlling the 27 level hybrid inverter has been proposed in which pulse width modulation is no longer needed. In this method, the resulting waveform will have the desired total Harmonic Distortion and the closest form to the ideal sinus.

Keywords: Neutral Point Diode Clamped Inverter, Sinusoidal pulse width Modulation, Phase Shifted Pulse Width Modulation, Total Harmonic Distortion.

I. INTRODUCTION

Electrical networks are faced with the challenge of interfering harmonics due to the increasing use of inverters. Increased use of such transducers requires providing more efficient ways to weaken the harmonic components. Using multilevel inverters instead of two level inverters is a method of improving the periodic waveform through increasing the output voltage steps. This method provides a better waveform and almost solves the problem. There exist various types of multilevel inverters, which can provide certain number of voltage steps in the output.

Obviously, greater number of output steps results in smoother variation of the waveform with respect to time and it would have a greater resemblance to the continuous waveform. Accordingly, two common types of multilevel inverters called Five-level Neutral Point Diode Clamped Inverter and 27-level hybrid inverters can be introduced each of which providing different harmonic quality based on their switching method. The most common switching technique is sinusoidal pulse width modulation technique.

In this method instead of having a constant output in period of each level, the level is sequentially sampled by comparing high frequency triangular signal and sinusoidal reference signal. The other method similar to the previous technique is the shifted pulse width modulation in which multiple triangular carriers are used, each of which is unique to a particular level. The method presented in this paper is based on tracking the reference signal. The inverter output will track an ideal sinusoidal waveform without using a carrier signal. The present paper describes the result of applying the mentioned methods on these inverters. Through comparing the harmonic results of output waveforms for each method, a proper vision for the corresponding topic will be provided.

II. FIVE-LEVEL NEUTRAL POINT DIODE CLAMPED INVERTER

A. General Structure

The structure of this inverter is shown in Figure 1. The input DC voltage is divided into equal sections using even number of capacitors. The voltage of each section is transferred to load in a proper time using the corresponding switch. The required equipment for realization of this structure are:

$$\begin{cases} m-1: \text{Number of Capacitors} \\ 2(m-1): \text{Number of Switches} \\ (m-1)(m-2): \text{Number of neutral point diode clamp} \end{cases} \quad (1)$$

where, m is the number of desired output levels. So in order to have five-level inverter, 4 number of capacitors, 4 number of switches and 12 number of diodes are required. The applied reverse voltage that diodes must endure on each branch determines number of diodes in that branch. According to Figure 1, reverse voltage on a branch with three diodes is 3 times greater than a branch, which has only one diode. This is also true for a two diode branch [4].

B. Control Method

Switching pattern of the inverter is shown in Table 1. Numbers 1 and zero indicate the on and off states of the switch respectively. The resulting output waveform from

simulation of Table 1 pattern with and without PWM is illustrated in Figures 2 to 4. The restriction of this structure is that the number of clamp diodes is a quadratic function of the output levels. Therefore, to achieve a greater number of steps, the number of clamping diodes experiences an unacceptable increase and restricts the use of this structure for waveforms with more steps and smoother variations.

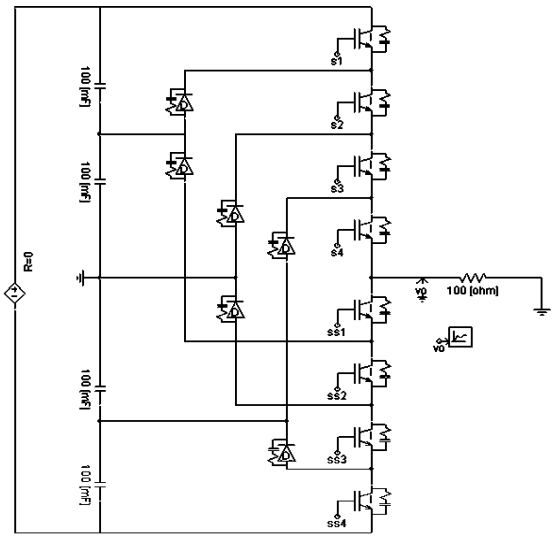


Figure 1. Structure of a five-level inverter with cutting diode

To create the desired pulse width modulation in this type of inverters, four-carrier signals are compared to reference signals. Consequently, the reference signal is divided into five separate sections as shown in Figure 3 and each section is sampled with its own carrier. Considering the fact that sinus has slow variations around the angles near 90 and its odd multiplies, the carrier frequency for these areas can be chosen lower than the angles near zero and integer multiplies of 180 [4].

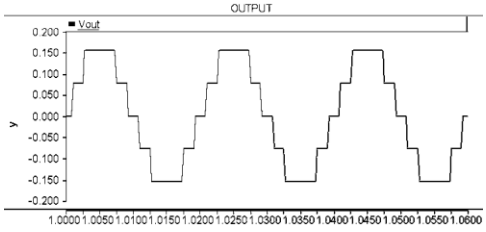


Figure 2. Simulation result of five-level cutting diode inverter

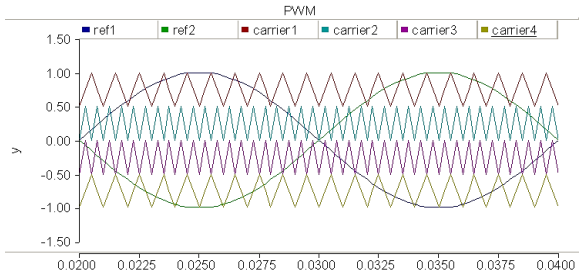


Figure 3. The pulse width modulation method for five-level Neutral Point Diode Clamped Inverter

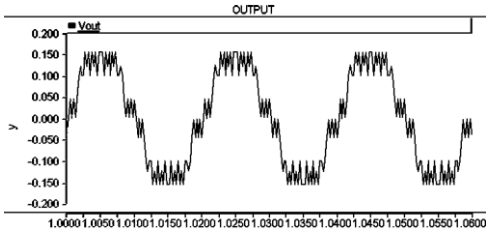


Figure 4. Simulation result of five-level Neutral Point Diode Clamped Inverter

Table 1. Switching patterns for achieving desired voltage levels in five-level cutting diode inverter output 1

V_{out}	S1	S2	S3	S4	S1′	S2′	S3′	S4′
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

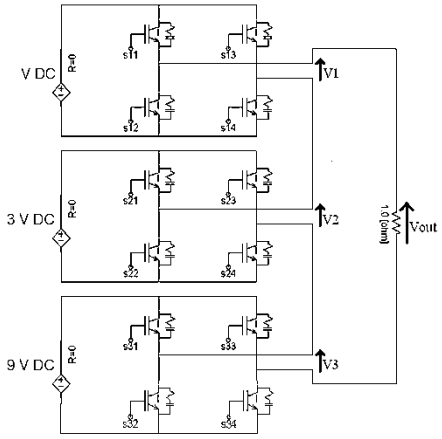


Figure 5. 27-level hybrid inverter structure

III. 27-LEVEL HYBRID INVERTER

A. General Structure

Another structure that can be proposed for increasing the number of voltage steps in the output is the 27-level hybrid inverter. This type of inverter, which is depicted in Figure 3, uses three DC sources with voltage ratio of 1/3/9 [5]. This inverter is composed of three distinct parts, each of which can viewed as a three-level inverter and has the ability of producing positive, negative and zero polarities in their output. Table 2 illustrates the different types of switch arrangements for producing these polarities and their voltage. Finally, each of these polarities will appear on the output of each H-bridge cell.

The load voltage is generated by the algebraic summation of these voltages. Table 3 shows by which pattern a 27-level output voltage can be achieved [5]. Based on the mentioned arrangements in Tables 2 and 3 the control unit changes the switch states in equal time periods. Regarding the number of voltage steps *dv*/*dt* will decrease significantly compared to the 5-level inverter. The output of simulation has been illustrated in Figure 6.

Table 2. Polarity on each side of the 27-level hybrid inverter according to the turned on switches

Polarity	Active Switches	Voltage	Output
P	S11, S14	+1 V_{dc}	V_1
Z	S12, S14	0	
N	S12, S13	-1 V_{dc}	
P	S11, S14	+3 V_{dc}	V_2
Z	S12, S14	0	
N	S12, S13	-3 V_{dc}	
P	S11, S14	+9 V_{dc}	V_3
Z	S12, S14	0	
N	S12, S13	-9 V_{dc}	

Table 3. Generation of 27 voltage levels through combining different polarities of each part in 27-level hybrid inverter

V_3	V_2	V_1	V_{out}	V_3	V_2	V_1	V_{out}
P	P	P	+13	N	N	N	-13
P	P	Z	+12	N	N	Z	-12
P	P	N	+11	N	N	P	-11
P	Z	P	+10	N	Z	N	-10
P	Z	Z	+9	N	Z	Z	-9
P	Z	N	+8	N	Z	P	-8
P	N	P	+7	N	P	N	-7
P	N	Z	+6	N	P	Z	-6
P	N	N	+5	N	P	P	-5
Z	P	P	+4	Z	N	N	-4
Z	P	Z	+3	Z	N	Z	-3
Z	P	N	+2	Z	N	P	-2
Z	Z	P	+1	Z	Z	N	-1
Z	Z	Z	0	-	-	-	-

B. Investigation of Pulse Width Modulation Methods for 27-Level Hybrid Inverters

Two common methods of switching for mentioned inverters are sinusoidal pulse width modulation and phase shifted pulse width modulation [6, 7]. In addition, there exist a new method for controlling the inverter switching which will be described comprehensively.

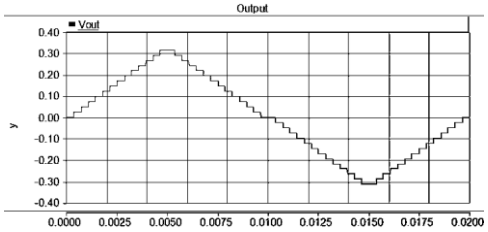


Figure 6. Simulation result of 27-level hybrid inverter

B.1. Sinusoidal Pulse Width Modulation

In order to preserve maximum modulation advantage in sinusoidal pulse width modulation technique, the amplitude of the triangular carrier signal is assumed to be identical with the reference signal amplitude. The control unit not only controls the required switch arrangements for achieving each of the 27 levels but also based on PWM principles and through comparing the reference and carrier signals defines the switching times for each level. The p criterion is defined as:

$$p = \frac{f_c}{2 f_0} \tag{2}$$

where, f_c is the carrier frequency and f_0 is the reference frequency. Fourier coefficients of the output voltage can be calculated using the following equations:

$$B_n = \sum_{m=1}^{2p} \left\{ \frac{4V_m}{m\pi} \sin\frac{n\delta_m}{4} \left[\sin n\left(\alpha_m + \frac{3\delta_m}{4} \right) - \right.\right.$$
$$\left.\left. - \sin n\left(\pi + \alpha_m + \frac{\delta_m}{4} \right) \right] \right\} \tag{3}$$

where, α_m is the starting angle of the mth positive paired pulses, δ_m is the pulse length and V_m represents the desired output voltage level while applying the mth pulse.

According to Equation (3) as the carrier frequency increases the sinus argument in sigma term will decrease due to reduction of δ_m. In addition, the number of the summation terms for calculating B_n, which are also responsible for harmonics creation, are reduced. Therefore, it is expected that the total harmonic distortion, which is calculated by Equation (4), decrease as the frequency carrier increases. This reduction has been illustrated in section four of the paper.

$$THD = \frac{1}{V_1} \sqrt{\sum_{n=2}^{\infty} V_n^2} \tag{4}$$

where, V_1 is the amplitude of the main component and V_n is the amplitude of the harmonic number n.

Figure 7 shows the modulation process of this inverter. In order to gain a better perception of the figure, lower carrier frequency is selected. However, final harmonic simulation results are based on high carrier frequency.

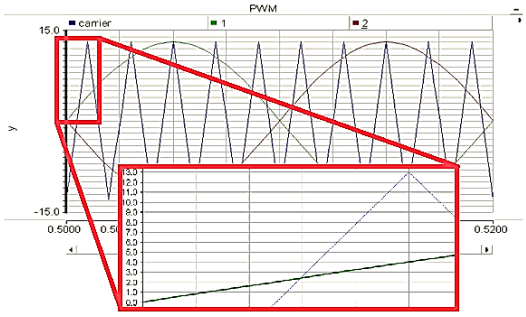


Figure 7. Sinusoidal pulse width modulation for 13 positive and 13 negative levels

B.2. Shifted Pulse Width Modulation

The shifted pulse width modulation technique requires equal number of carrier signals as output steps [7]. Therefore, for the mentioned inverter, 27 carrier signals with identical frequencies are required. The carrier signals have the phase shift of β_n with respect to the base carrier. In this case, for each level one of the carriers will take part in the modulation process. The β can be calculated from Equation (5).

$$\beta = \frac{360}{m} \tag{5}$$

where, m is the number of output levels.

Figure 9 shows two sample carrier signals. As can be seen, the phase difference between two triangular waves is equal to 6/43°. Other carriers will have the same phase shift with respect to the previous carriers. Therefore, once a level is started in the output, the carrier signal, which produces the corresponding PWM, will be started at the same time with zero phase delay. Thus, all levels will have

same state with respect to their carrier signal phase. The pulse width modulation will be symmetric for all levels and harmonic quality will further be improved.

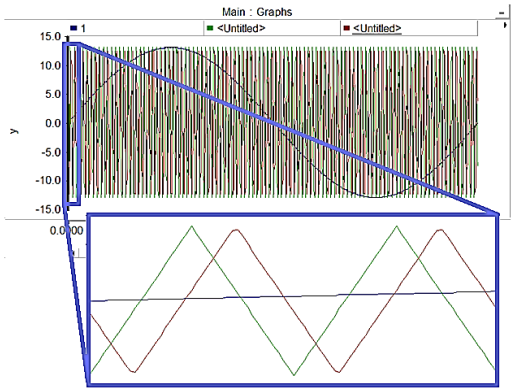


Figure 9. Two sample carrier waves by 5000 Hz

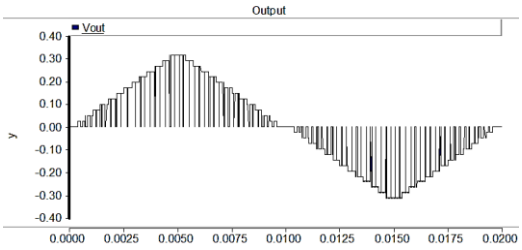


Figure 10. The result of 27-level hybrid inverter simulation by shifted PWM

C. A Novel Method for Controlling 27-Level Hybrid Inverter with Reference Signal Tracking

The presented method for controlling the switching operation of a 27-level hybrid inverter in this section is about tracking the reference signal without comparing it to the carrier signal. In addition, this method uses α-β conversion. In this method, the angle θ of the three-phase system must be calculated at any instant so that the instantaneous value of the reference signal can be calculated and the reference signal will be synchronous with the output [7]. This can be achieved using PLL and conversion of three phase to two α-β phases.

Phase lock unit, preserves the initial phase angle during the system operation. Using α-β conversion, three-phase system coordinates can be converted into a two phase system coordinates. The value of θ and instantaneous value of the reference voltage can simply be considered as the input information to the control unit. Then amplitude of the reference signal is divided into 13 equal parts. Each of these parts constitutes an amplitude unit. So 13 voltage levels is created in each positive and negative half cycles and voltage difference between each of these levels and the next or previous levels is equal to an amplitude unit.

At any given moment, the control unit compares the instantaneous value of the reference signal, which is calculated using α-β conversion to each of these 13 levels. Once it reaches a new level, control unit changes the arrangement of the switches to go to the next step based on Tables 2 and 3. Thus, unlike previous cases in which the rearrangement of the switches from one level to another was performed based on equal schedules, jumping to the next steps will occur at the instances which has a complete overlap with the sine wave. The α-β conversion is performed by the following equation:

$$\begin{bmatrix} V_\alpha & V_\beta \end{bmatrix}^T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} & V_{bn} & V_{cn} \end{bmatrix} \quad (6)$$

where, V_{an}, V_{bn} and V_{cn} are the voltages of a three-phase system.

After calculating the two-phase components, three phase system angle θ and the amplitude of the reference signal is obtained from the following equations:

$$|V| = \sqrt{V_\alpha{}^2 + V_\beta{}^2} \quad (7)$$

Therefore, the reference signal can be recovered if its amplitude and phase are known. Horizontal lines in Figure 11 represent the amplitude units. Once sinus wave passes each of these units, the output waveform will jump to the next level. Figure 12 shows one cycle of the output.

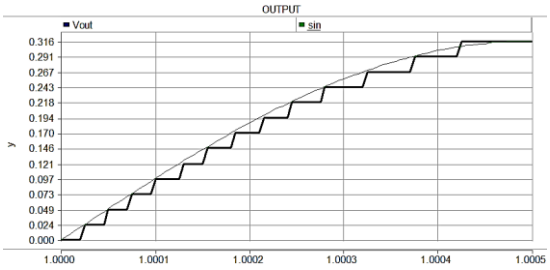


Figure 11. A quarter of the full cycle of simulation output

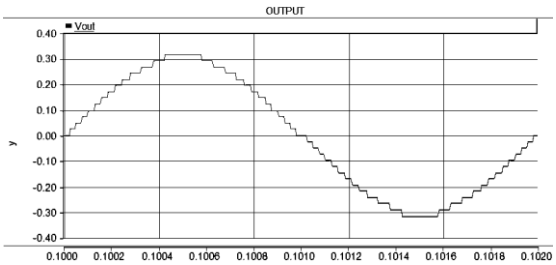


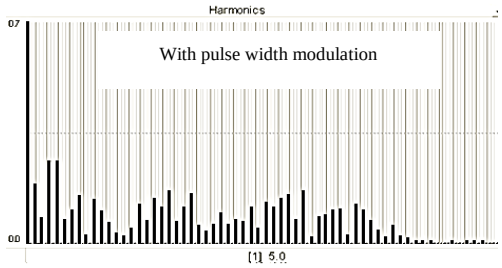
Figure 12. Simulation results for 27-level hybrid inverter with a new control method

IV. INVESTIGATING OF HARMONIC RESULTS

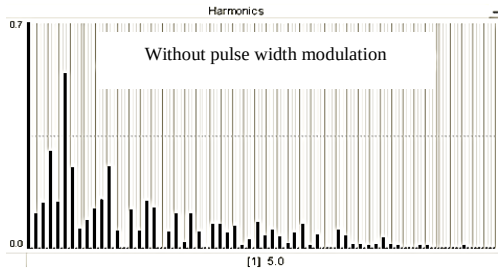
Figure 13 shows harmonic spectrum of the five-level Neutral Point Diode Clamped Inverter up to 127 for two cases of with PWM and without PWM. Magnification of figures are 5x which means that the main component is 5 p.u. and it is drawn to 0.7 p.u. Comparing these two figures shows that the pulse width modulation results in attenuation of the lower-order components amplitude and amplification of the higher order harmonics.

So in case of applying an appropriate high frequency filter, proposed PWM technique can be viewed as a proper method for switching. Figure 14 shows the harmonic spectrum of the 27 level hybrid inverter using sinusoidal pulse width modulation technique with carrier frequencies of 1, 3 and 5 kHz. In addition, it shows the phase shift pulse width modulation in carrier frequency of 5 kHz.

Represented results are for the first 31 harmonics and magnification of figures is again 5*x*. The main component has been drawn to 1.2 pu. Given the short period of each level in the output, higher carrier frequency results in further attenuation of the components and harmonic quality improvement.

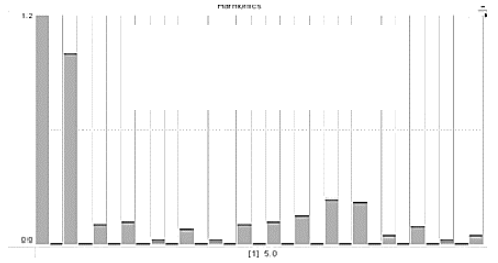


(a)

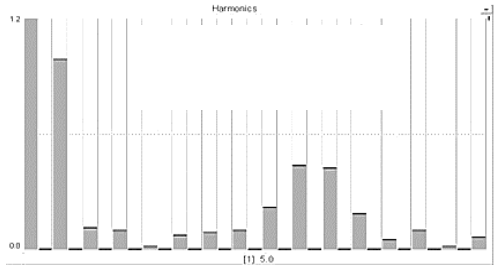


(b)

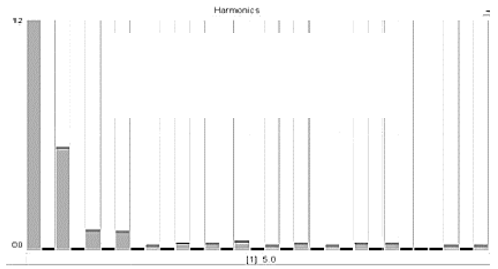
Figure 13. Harmonic spectrum of the five-level Neutral Point Diode Clamped Inverter, (a) With pulse width modulation, (b) Without pulse width modulation



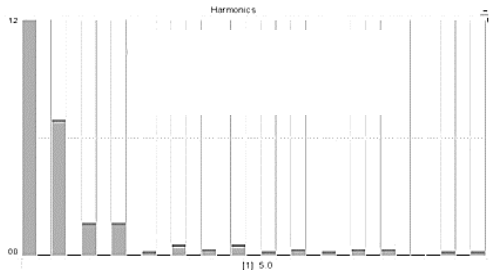
(a)



(b)



(c)



(d)

Figure 14. Harmonic spectrum of hybrid inverter with different switching methods, (a) Sinusoidal pulse width modulation with carrier 3 kHz, (b) Sinusoidal pulse width modulation with carrier 1 kHz, (c) Pulse width modulation with shifted pulse carrier 5 kHz, (d) Sinusoidal pulse width modulation with carrier 5 kHz

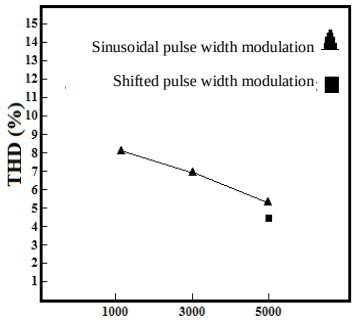
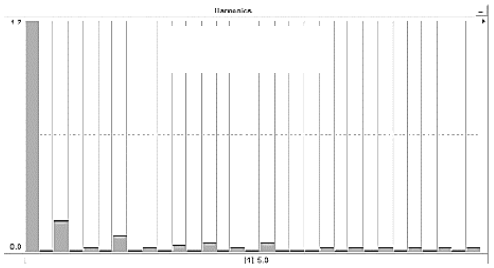
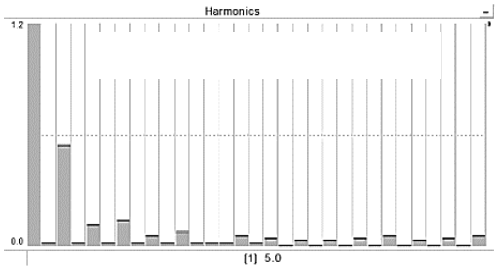


Figure 15. Output wave *THD* in hybrid inverter with different switching methods

The best harmonic spectrum achieved belongs to shifted pulse width modulation. Further improvement is also possible if the new method presented for 27 level inverter switching is used. As can be seen from Figures 16 and 17, if the new method is used, harmonic quality of the output will be improved and total harmonic distortion will be less than 2 percent.



(a)



(b)

Figure 16. Comparing the harmonic spectrum of hybrid inverter in different switching methods, (a) Proposed method, (c) Shifted pulse width modulation

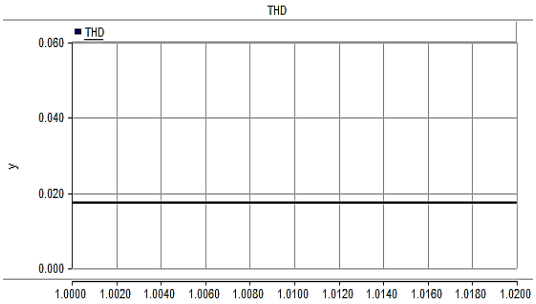


Figure 17. Output wave *THD* for hybrid inverter using new switching technique

V. CONCLUSIONS

Multilevel inverters by generating smoother variations in the output will further attenuate the disturbed harmonics on the grid side. It has been seen in this paper that different switching methods applied to two types of such inverters result in different harmonic qualities. Although the five level Neutral Point Diode Clamped Inverter has smoother changes compared to the simple 3- level inverter but it still requires a proper pulse width modulation to improve its harmonic spectrum.

Investigating the switching methods for 27-level hybrid inverter indicated that in sinusoidal pulse width modulation technique as the carrier wave frequency increases, harmonic spectrum and total harmonic distortion are improved due to the faster sampling of the signal. However, since the single carrier signal performs asymmetric sampling for different layers, shifted pulse width modulation has been proposed.

It was observed that due to the use of a separate signal carrier for each level, a symmetric sampling is performed for each level pair and output waveform has a better harmonic state even in comparison with the best single carrier sinusoidal pulse width modulation. In the novel switching method for 27-level inverter, the output waveform is so close to the ideal sinus wave that the total harmonic distortion coefficient is about 1 or 2 percent.

REFERENCES

[1] M. Azab, "Harmonic Elimination in Three-Phase Voltage Source Inverters by Particle Swarm Optimization", Journal of Electrical Engineering & Technology Vol. 6, No. 3, pp. 334-341, 2011.

[2] S. Khomfoi, L.M. Tolbert, "Multilevel Power Converters", Power Electronics Handbook, Second Edition Elsevier, ISBN 978-0-12-088479, Chapter 17, pp. 451-482, 2007.

[3] A. Radan, A.H. Shahirinia, M. Falahi, "Evaluation of Carrier-Based PWM Methods for Multilevel Inverters", IEEE Industrial Electronics Int. Symposium, pp. 389-394, 2007.

[4] P. Purkait, R.S. Sriramakavacham "A New Generalized Space Vector Modulation Algorithm for Neutral Point Clamped Multilevel Converters", Progress in Electromagnetic Research Symposium, Cambridge, USA, pp. 26-29, March 2006.

[5] E. Babaei, S.H. Hosseini, G.B. Gharehpetian, M.T. Haque, M. Sabahi, "Reduction of DC Voltage Sources and Switches in Asymmetrical Multilevel Converters Using a Novel Topology", Electric Power Systems Research, Vol. 77, pp. 1073-1085, 2007.

[6] Y.S. Lai, F.S. Shyu, "Topology for Hybrid Multilevel Inverter", IEE Proceedings on Electric Power Applications, Vol. 149, pp. 449-458, 2002.

[7] L. Saribulut, M.E. Meral, A. Teke, M. Tumay, "Performance Comparison of PWM Methods for 27-Level Hybrid Multilevel Inverters", Gazi University Journal of Science, GUJ Sci, Vol. 25, No. 3, pp. 689-695, 2012.

[8] S. Jeevananthan, R. Nandhakumar, P. Dananjayan, "Inverted Sine Carrier for Fundamental Fortification in PWM Inverters and FPGA Based Implementations", Serbian Journal of Electrical Engineering, Vol. 4, pp. 171-187, 2007.

[9] M. Nilkar, E. Babae, M. Sabahi, "A New Single-Phase Cascade Multilevel Inverter Topology Using Four-Level Cells", Published in Electrical Engineering (ICEE), 20th Iranian Conference, pp. 448-353, 2012.

BIOGRAPHIES

Alireza Pirouznia received his B.Sc. degree in Electrical Engineering from University of Tabriz, Iran in 2011. Currently, he is a M.Sc. student of Power Engineering in Seraj Higher Education Institute, Tabriz, Iran. He has teaching experience in power system analysis, electrical machinery and theory of electrical circuits as teaching assistant at Seraj Higher Education Institute, Tabriz, Iran from 2012 to 2013. His interests include power electronics converters and distributed generation.

Hojat Hatami received his B.Sc., M.Sc. and Ph.D. degrees in Electrical Engineering from University of Tabriz, Iran in 2005, 2008 and 2014, respectively. In 2010, he joined the Department of Electrical Engineering at Seraj Higher Educational Institute, Iran, and now, he is Head of Power Engineering Department of this university. He is teaching electrical machinery, power electronics, technical English, and electrical installations at Seraj Higher Education Institute. He has a lot of research in power engineering such as electrical machinery, motor drives, power system protection, power quality, FACTS controllers, and mathematical methods in electrical engineering.

Naser Mahdavi Tabatabaei was born in Tehran, Iran, 1967. He received the B.Sc. and the M.Sc. degrees from University of Tabriz (Tabriz, Iran) and the Ph.D. degree from Iran University of Science and Technology (Tehran, Iran), all in Power Electrical Engineering, in 1989, 1992, and 1997, respectively. Currently, he is a Professor in International Organization of IOTPE. He is also an academic member of Power Electrical Engineering at Seraj Higher Education Institute (Tabriz, Iran) and teaches power system analysis, power system operation, and reactive power control. He is the General Chair of International Conference of ICTPE, Editor-in-Chief of International Journal of IJTPE and Chairman of International Enterprise of IETPE all supported by IOTPE. He has authored and co-authored of six books and book chapters in Electrical Engineering area in international publishers and more than 135 papers in international journals and conference proceedings. His research interests are in the area of power quality, energy management systems, and power networks smart grid. He is a member of the Iranian Association of Electrical and Electronic Engineers (IAEEE).

Ali Jafari was born in Zanjan, Iran in 1988. He received the B.Sc. degree in Power Electrical Engineering from Abhar Branch, Islamic Azad University, Abhar, Iran in 2011. He is currently the M.Sc. student in Seraj Higher Education Institute, Tabriz, Iran. He is the Member of Scientific and Executive Committees of International Conference of ICTPE and also the Scientific and Executive Secretary of International Journal of IJTPE supported by International Organization of IOTPE (www.iotpe.com). His research fields are intelligent algorithms application in power systems, power system dynamics and control, power system analysis and operation, and reactive power control.