International Journal on
"Technical and Physical Problems of Engineering"
(IJTPE)
Published by International Organization of IOTPE

ISSN 2077-3528
IJTPE Journal
www.iotpe.com
ijtpe@iotpe.com

June 2016 | Issue 27 | Volume 8 | Number 2 | Pages 40-45

DVR CONTROL FOR BALANCED AND UNBALANCED SAG MITIGATION

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Abstract- Voltage sags are the most regular power quality problem that occurs in power system. Load performance degrades if they are subjected to sag. In this paper, to mitigate voltage sag, series compensation using battery-supported Dynamic Voltage Restorer is proposed. Reference generation algorithm for compensating both balanced and unbalanced sag is discussed and implemented. Hysteresis controller is employed to control the output of restorer. MATLAB/Simulink environment is used to for simulation of the system.

Keywords: Series Compensation, Balanced Sag, Unbalanced Sag, d-q Theory, Hysteresis Control.

I. INTRODUCTION

The installation of large number of non-linear electronic devices as well as the sudden disturbing events in power system leads to various PQ problems. These PQ problems is distorting the nature of supply waveform and hence degrades the performance of sensitive loads like electrical drives, computer systems etc. further impinging the economic loss to industrial customers. PQ problems include disturbances like transients, sag, swell, interruption, harmonics, flicker etc. Voltage sag is the commonly occurring disturbance. Voltage sag is a decrease in root mean square value of supply voltage at power frequency between 0.9 pu to 0.1 pu for duration of half cycle to 1 minute [1]. So, reduction in supply voltage may cause tripping of sensitive loads by means of protection circuit and can stall the industrial processes. Solution to this problem is that load must not experience these disturbances in power system.

To mitigate PQ problems various devices emerged which were commonly named as CPD. CPD technology includes shunt, series as well as combination of shunt and series compensating devices. DVR is a member of CPD technology and is a series compensating device. DVR injects voltage in series with the supply voltage of estimated magnitude and frequency [2-3].

Voltage sags can occur at the starting of heavy three-phase loads like induction motor which results into balanced sag or it can occur due to some unsymmetrical fault like line-to-ground fault which results into unbalanced sag. [4, 5]. DVR must restore the voltage on the load side to the desired amplitude and waveform when the sag occurring is of balanced or of unbalanced nature. DVR consists of:

a) Power circuit: It includes VSI, D.C. supply storage and injection transformer.

b) Control circuit: It includes the algorithm implemented, controller to control the VSI output and the monitoring system. The single phase equivalent scheme for DVR is as shown in Figure 1.

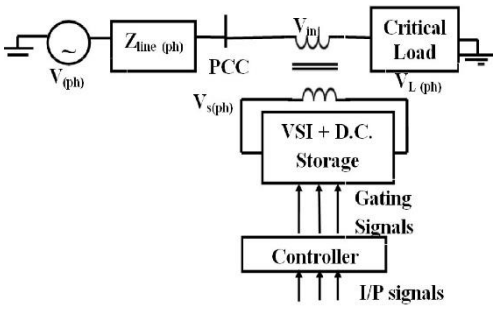

Figure 1. Single phase DVR equivalent circuit

DVR is realized as a voltage source by using VSI [6]. The transformer is connected in series with the incoming supply lines and thus it act as an isolation between supply source and DVR. The battery is connected along with the energy storage capacitor as a D.C. energy source for VSI. An LC filter is connected to eliminate the higher order switching harmonics. Inductance of injection transformer windings acts as L_f and C_f is connected across secondary on line side. Thus phase voltage at PCC and load phase voltage is given by Equations (1) and (2), respectively.

$$\overline{V_{s(ph)}} = \overline{V}_{(ph)} - \overline{I}.\overline{Z_{line(ph)}} \quad (1)$$

$$\overline{V_{L(ph)}} = \overline{V_{s(ph)}} + \overline{V_{inj(ph)}} \quad (2)$$

where, $\overline{V_{s(ph)}}$ is source voltage, I is the line current and $\overline{V_{inj(ph)}}$ is the series injected voltage.

Load characteristics can affect the control strategy as some loads can be sensitive to change in voltage magnitude while some load can be sensitive to phase angle jumps [7]. The $\overline{V_{inj(ph)}}$ should be in quadrature with I for optimal utilization of energy stored and minimum active power consumption [6]. Many researches were carried out in the field of design and control of DVR, optimizing the energy utilization, compensation strategies, their analysis at simulation as well as experimental level and various topologies of DVR [8-11]. This paper proposes two-step technique for DVR control. First step is of voltage reference generation using synchronous reference frame (d-q) theory and second step is implementing PWM technique to control V_{inj}.

II. REFERENCE SIGNAL GENERATION SCHEME

The load voltage compensation scheme in this paper tracks the reference voltage for each phase. The algorithm for reference voltage generation is based on conversion of time-domain phase-to-ground voltage signals into an equivalent d-q domain signals using Park's transformation as shown in Equation (3) and vice-versa using inverse Park's transformation using Equation (4) [12-13].

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \sin(\theta\text{-}120^\circ) & \sin(\theta\text{+}120^\circ) \\ \cos(\theta) & \cos(\theta\text{-}120^\circ) & \cos(\theta\text{+}120^\circ) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \cos(\theta) \\ \sin(\theta\text{-}120^\circ) & \cos(\theta\text{-}120^\circ) \\ \sin(\theta\text{+}120^\circ) & \cos(\theta\text{+}120^\circ) \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (4)$$

where v_a, v_b, v_c are instantaneous values of phase voltages and v_d, v_q are their equivalent d-q components.

A. Balanced Sag

As the voltage sag is balanced with no distortion, it contains only positive sequence component. The schematic to compose the voltage reference for balanced sag is as shown in Figure 2.

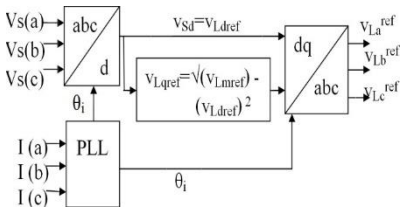

Figure 2. Reference generation schematic

The PCC phase voltage signals $v_{s(a)}, v_{s(b)}, v_{s(c)}$ are converted to v_{sd} using Equation (3). The sine and cosine vectors are obtained by using PLL over line current. Thus, d-component obtained, is steady. Hence it is a reference d-component v_{Ld}^{ref} of desired load voltage $v_{L(ph)}^{ref}$. The q-component of $v_{L(ph)}^{ref}$, v_{Lq}^{ref} is calculated using Equation (5).

$$v_{Lq}^{ref} = \sqrt{(v_{Lm}^{ref})^2 - (v_{Ld}^{ref})^2} \quad (5)$$

where, v_{Lm}^{ref} is the peak value of load reference voltage. Reference load phase voltages $v_{La}^{ref}, v_{Lb}^{ref}, v_{Lc}^{ref}$ are then obtained from $v_{Ld}^{ref}, v_{Lq}^{ref}$ by using Equation (4).

B. Unbalanced Sag

Due to unbalance in sag, d-component of PCC voltage v_{sd} consists of harmonics as well as inter-harmonics [14-16]. It is given by Equation (6) as

$$v_{sd} = v_{sd(const)} + v_{sd(\text{var})} \quad (6)$$

where, v_{sd}^{constt} is a steady component and v_{sd}^{var} is the fluctuating component. Thus, it is passed through an LPF to eliminate v_{sd}^{var}. The v_{sd}^{constt} refers to amplitude of fundamental PCC voltage, v_{sm}^{f}.

Phase voltage fundamental components $v_{s(a)}^{f}, v_{s(b)}^{f}, v_{s(c)}^{f}$ are computed using Equation (7). These fundamental components are then processed using the scheme shown in Figure 2 to compose reference load voltages, $v_{L(a)}^{ref}, v_{L(b)}^{ref}, v_{L(c)}^{ref}$.

$$\begin{bmatrix} v_{s(a)}^{f} \\ v_{s(b)}^{f} \\ v_{s(c)}^{f} \end{bmatrix} = v_{sm}^{f} \begin{bmatrix} \sin(\theta) \\ \sin(\theta\text{-}120^\circ) \\ \sin(\theta\text{+}120^\circ) \end{bmatrix} \quad (7)$$

C. Hysteresis Control

Hysteresis control is a non-linear PWM technique which can be used for controlling the output of VSI [17]. The input to this type of controller is limited within a band by means of switching the states of VSI. It utilizes the feedback of $v_{s(a)}, v_{s(b)}, v_{s(c)}$ to generate the error signal, $v_{L(ph)}^{err}$, given by (8) for each phase.

$$v_{L(ph)}^{err} = v_{L(ph)}^{ref} - v_{s(ph)} \quad (8)$$

This signal is fed as an input to controller and is compared with pre-defined constant value of hysteresis band '*h*', to generate the gating signals for switches of VSI. The *h* is fixed for desired switching frequency f_{sw} of VSI [18]. The switching logic is as given in Table 1.

III. SIMULATION OF DVR

DVR performance can be observed by considering various supply conditions of source [19]. In this work, MATLAB/Simulink environment along with Power System Toolbox is used to simulate DVR. Three phase programmable voltage source is used to simulate sag conditions. The Simulink model is shown in Figure 3.

A. Power Circuit

H-bridge type VSI is realized using four IGBTs as power switches for load voltage compensation in each phase. Battery (V_{dc}) along with common D.C. link capacitor (C_{dc}) is provided to H-bridge.

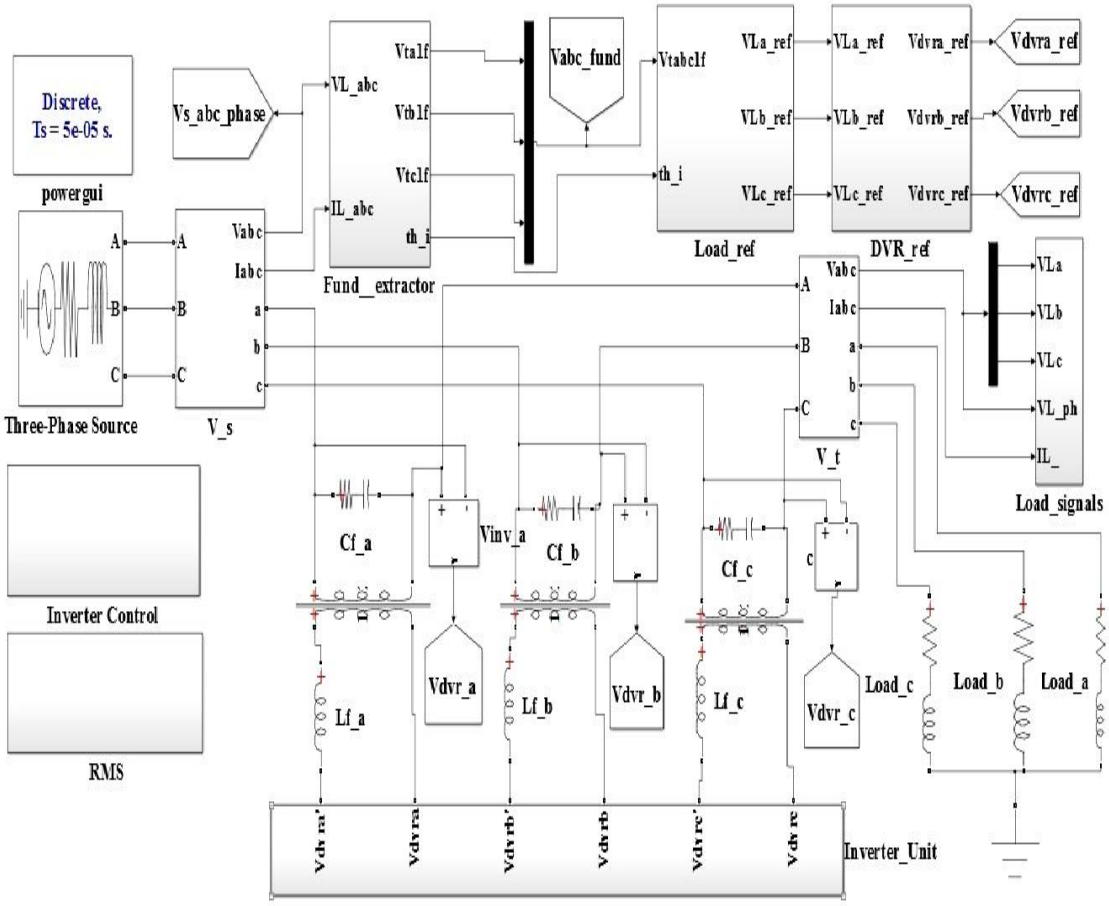

Figure 3. Simulink model

Single-phase injection transformer is connected to H-bridge in each phase on primary side and corresponding phase line on transformer's secondary side. Three single phase inductive type load are connected with a common ground.

B. Control Circuit

Two-level hysteresis PWM control is implemented by employing separate controller for each VSI. The error signal given by equation (8) is fed as input to the hysteresis controller. The switching logic as realized for H-bridge switches in Table. 1 changes the state of VSI between $+V_{dc}$ and $-V_{dc}$ and hence control the series injected voltage by DVR.

The simulated controller for phase '*a*' in the designed model is as shown in Figure 4. Logical controller for phase '*b*' and phase '*c*' are simulated in a similar way for VSI control in phase '*b*' and '*c*', respectively.

IV. RESULTS

In simulation, load is fed by balanced three phase supply. The simulation time of 0.6 second is fixed. The load voltage is to be regulated at rms. value of 230 V. To understand the effect of voltage injection by DVR using proposed algorithm, both balanced and unbalanced sag is created in duration of 0.2 sec to 0.5 sec. The simulation data is given in Appendix 2.

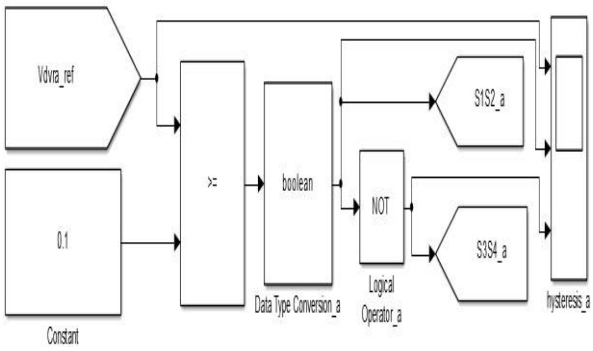

Figure 4. Hysteresis controller

A. Balanced Sag

Condition of balanced voltage sag at PCC is simulated as shown in Figure 5. Reduction in phase voltage V_S at 0.7 pu for phase *a*, *b* and *c* occurs at 0.2 second. Sag mitigation scheme is implemented as shown in Figure 2. The voltage signal at fundamental frequency is extracted and hence the reference signal of rated load voltage is synthesized by implementing reference generation algorithm.

The error voltage of each phase is then fed to their respective hysteresis controller of VSI. Thus, VSI acts as a voltage source and injects estimated voltage and hence regulates the load voltage V_L at rated value as in Figure 5.

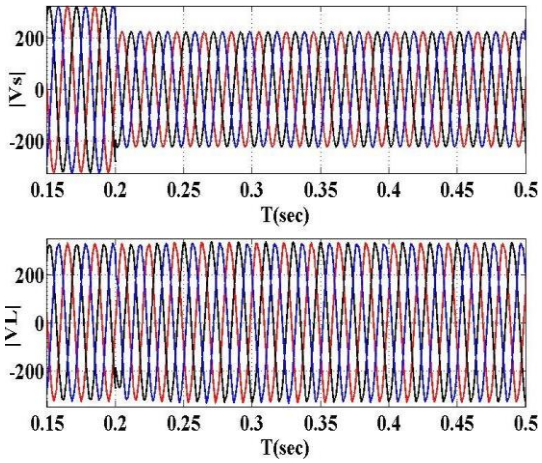

Figure 5. Balanced sag and its mitigation

Thus, sag at PCC is not experienced by load. Effective voltage compensation by proposed algorithm can be observed from the r.m.s voltage profile of voltage at PCC V_{srms} and load voltage V_{Lrms} as shown in Figure 6. It can be seen that V_{srms} exhibits the sag but V_{Lrms} value is regulated around 230 V.

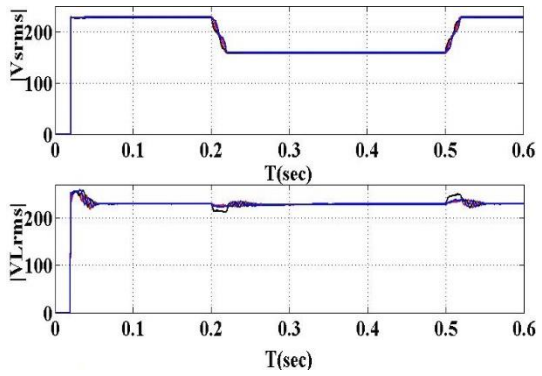

Figure 6. The rms profile of balanced sag

B. Unbalanced Sag

An unbalanced sag condition is simulated by considering unequal magnitude of phase voltages. Voltage sag occurs in phase b and c at 0.2 sec. Such unbalanced condition is simulated as shown in Figure 7. Thus, by implementation of proposed DVR control technique, sag is mitigated and hence load voltage becomes regulated as can be seen from Figure 7.

The rms voltage profile is as shown in Figure 8. It depicts the unbalanced V_{srms} for each phase. The implementation of scheme is proved as V_{Lrms} is regulated at around 230 V rms in sagged phases.

V. CONCLUSION

Power Quality problem is a critical issue faced by the industries forcing them into economical loss. Voltage sag is a frequently occurring power quality issue. It results in deficiency of supply voltage and hence affects load performance. DVR is a custom power device that injects voltage in series.

Balanced sag or unbalanced sag can occur in power system which may affect the load performance. To control DVR for sag mitigation, d-q theory has been implemented. The reference generation scheme utilizes d-q conversion and composes the reference voltage waveforms of desired peak voltage for balanced as well as unbalanced sag. The proposed reference generation scheme along with hysteresis control track the reference voltage by means of VSI as a voltage source and thus compensates the load voltage. The load voltage is regulated at rated load voltage and hence improves load performance.

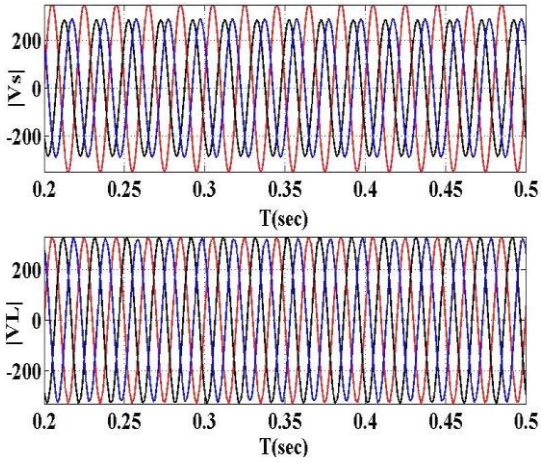

Figure 7. Unbalanced sag and its mitigation

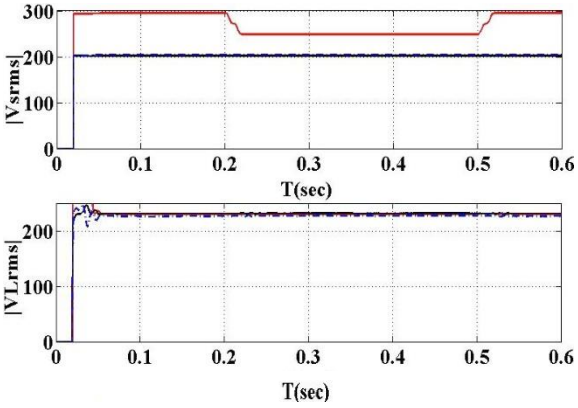

Figure 8. The rms profile of unbalanced sag

APPENDICES

Appendix 1. Hysteresis Control Switching Law

Tables 1 represent the switching logic of inverter using hysteresis control.

Table 1. Switching logic of VSI

Comparison of error	ON switches	OFF switches	$+V_{dc}/-V_{dc}$
$V_{L(ph)}^{err} \geq h$	S_1, S_2	S_3, S_4	$+V_{dc}$
$V_{L(ph)}^{err} < h$	S_3, S_4	S_1, S_2	$-V_{dc}$

Appendix 2. Simulation Data

Source line voltage = 415 V; Battery storage voltage = 200 V; D.C. link capacitor = 4700 µF; Filter inductance = 7 mH; Filter capacitor = 150 µF; Sampling frequency = 20 kHz; Maximum switching frequency = 5000 Hz; Hysteresis band = 5 V.

NOMENCLATURES

PQ: Power Quality
CPD: Custom Power Device
DVR: Dynamic Voltage Restorer
VSI: Voltage Source Inverter
PCC: Point of Common Coupling
LPF: Low Pass Filter
PWM: Pulse Width Modulation
IGBT: Insulated Gate Bipolar Transistor
rms.: Root Mean Square
D.C.: Direct Current
ph: Phase *a*, *b* and *c*
d-q: Direct-Quadrature
L_f: Filter Inductor
C_f: Filter Capacitor
pu: Per Unit
h: Error tolerance value
f_{sw}: Maximum Switching frequency
V_{dc}: D.C. energy battery storage
C_{dc}: D.C. link capacitor
R-L: Resistive-Inductive load
T_s: Sampling time

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