International Journal on
"Technical and Physical Problems of Engineering"
(IJTPE)
Published by International Organization of IOTPE

ISSN 2077-3528
IJTPE Journal
www.iotpe.com
ijtpe@iotpe.com

March 2023 | Issue 54 | Volume 15 | Number 1 | Pages 271-282

31-LEVEL SINGLE-PHASE CASCADED INVERTER WITH MINIMAL COMPONENT COUNT

S.N. Tackie [1] N.M. Komi [1] O.C. Ozerdem [2]

1. Department of Electrical and Electronic Engineering, Near East University, Nicosia, Northern Cyprus
samuel.niitackie@neu.edu.tr, komimarvin@gmail.com
2. Electrical and Electronics Engineering Department, European University of Lefke, Lefke, Northern Cyprus
oozerdem@eul.edu.tr

Abstract- This work proposes a group of new cascaded single-phase multilevel inverter topologies. The proposed cascaded topologies are based on a string connection of a number of submultilevel units and they generate only positive output voltage. Therefore, an H-bridge is required to generate both positive and negative output voltage. Among the proposed topologies is a 31-level single-phase inverter composed of two cascaded submultilevel units and an H-bridge. The proposed 31-level single-phase inverter is realized with minimum component count i.e., 4 dc sources, 12 unidirectional semiconductor switches and driver circuits respectively. The major advantages of the proposed topology are better output waveforms, generation of higher levels of output voltage with less component count, less complex cascaded structure, reduced power losses and the utilization of lower rated switches. To validate the superiority of the proposed multilevel inverter, comparative analysis of existing topologies and the proposed inverter are investigated. Also, symmetric and asymmetric characteristics of the input voltages are analyzed. Finally, the proposed multilevel inverter is built and simulated in EMTDC/PSCAD software. Simulation results validates the theoretical analysis.

Keywords: Asymmetric Multilevel Inverter, Basic Unit, Fundamental Frequency Control, Submultilevel.

1. INTRODUCTION

Multilevel inverters (MLI) continue to receive maximum attention because they are the preferred applicable inverter topology for medium power and high-power systems. Multilevel inverters offer several advantages such as reduced THD content, minimum harmonic content, reduced switching losses, minimum electromagnetic interference, reduced voltage stress on switches, utilization of lower rated switches, high efficiency, better output waveforms and are suitable for medium and high-power systems [1-2]. Also, multilevel inverters are suitable for application in DVR, photovoltaics, electric vehicles, FACTS, electrical drives, active power filters etc. [3-7].

Various multilevel inverter topologies have been developed over the years. However, there are three conventional topologies namely FC (flying capacitor), NPC (Neutral-point clamped) and CHB (cascaded H-bridge) multilevel inverters. Additionally, there are prominent topologies such as Hybrid and Modular MLI topologies [8]. These topologies are easily controlled by any of the following PWM techniques; multi-carrier, single pulse, sinusoidal, space vector, third harmonic and fundamental frequency control [9]. Limitations of FC and DC MLI topologies are the high number of capacitors and diodes they require respectively, unbalanced DC link states and device voltage magnitude. These limitations are absent in CHB topology but also requires high quantities of dc sources and power switches [10-11]. With respect to input voltage magnitudes, MLI are classified into symmetrical MLI where the input voltages are equal and asymmetrical MLI where the input voltages are unequal. The latter topology generates higher step output voltage compared to symmetrical MLI [12].

The focus of researchers in the past few years and recently is to improve the architecture of MLI topologies placing more emphasis on efficiency, minimizing THD and reducing the overall component count especially switches, dc sources and driver circuits while concurrently expanding the levels of output voltage [14-16].

A new single-phase 31-level cascaded MLI is proposed in this research. The proposed inverter is derived with less component quantity i.e., semiconductor power switches, dc sources and driver circuits. The proposed topology offers superior advantages over some selected issued topologies. The rest of this article is segmented into the following parts; section 2 presents proposed basic and submultilevel units, cascaded structure using submultilevel units, symmetric and asymmetric analysis of the dc sources. Proposed 31-level topology is presented in section 3. Fundamental frequency control technique is presented in segment 4. Comparative analysis of the proposed topology and existing topologies are existing topologies are presented in segment 5. Results of simulation and conclusion are presented in segments 6 and 7 accordingly.

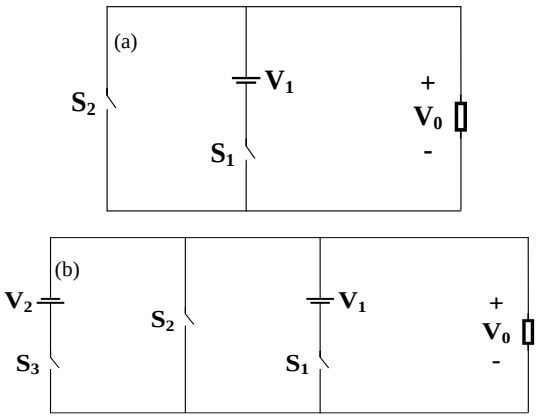


Figure 1. Basic units of the proposed MLI

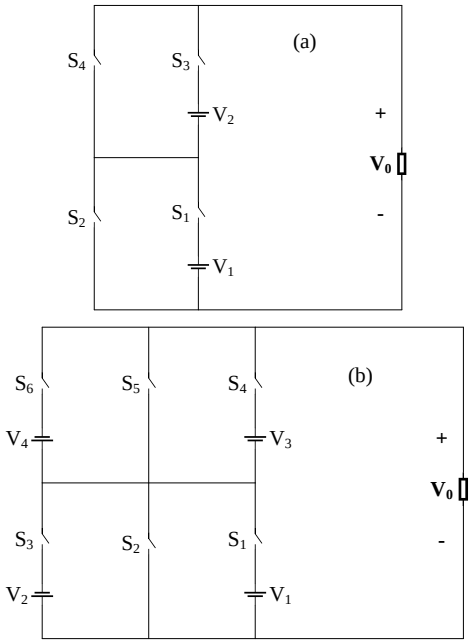
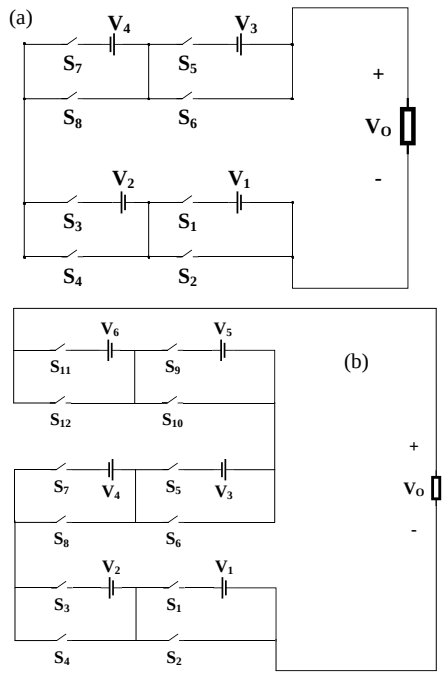


Figure 2. Sub-multilevel inverter topologies



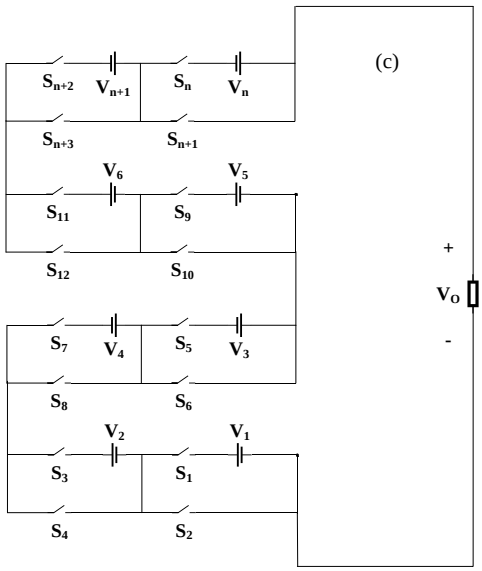


Figure 3. Various cascaded structures of the proposed inverter

2. PROPOSED MLI TOPOLOGIES

The basic units of the proposed single-phase multilevel inverter are illustrated by Figure 1. Figure 1a is made-up of one dc source and two power switches (unidirectional). Adding one dc source and one switch to the circuit of Figure 1a will produce the new circuit of Figure 1b capable of generating positive and negative output voltages. Both dc sources must be equal in magnitude. Figure 2 shows the submultilevel units. It is derived by series connection of two basic units. Figure 2a has two dc sources and four unidirectional switches while Figure 2b has four dc sources and six semiconductor switches. If *n* represent each basic unit of Figure 1, then the structures of Figure 2 are expressed by 2*n* accordingly. Figure 1a generates 1-level of positive output voltage while Figure 1b generates 3-levels of ($+V_1$, 0, $-V_2$) output voltages. Figure 2a generates 3-levels of positive output voltages and Figure 2b generates 5-levels of (negative and positive) output voltages.

An H-bridge structure is required by the topologies of Figure 1a and Figure 2a to generate negative output voltage. With respect to *n*, the dc source count and switch count for Figures 1a and 2a are computed by Equations (1) and (2) accordingly, where Q_{VDC} and Q_{SW} represent the quantity of dc sources and switches accordingly. Figure 3 shows various cascaded topologies using the submultilevel units of Figure 2a. Each cascaded topology generates only positive step output voltage. Figure 3a and Figure 3c generates 15-levels and 63-levels of positive step output voltage if asymmetric input voltages are utilized. Theoretical step waveform (positive 15-levles) of the proposed MLI is illustrated below by Figure 4.

For n =1

$$\begin{cases} Q_{V_{dc}} = n \\ Q_{S_w} = n \end{cases} \quad (1)$$

For n = 2

$$\begin{cases} Q_{V_{dc}} = n \\ Q_{S_w} = 2n \end{cases} \quad (2)$$

2.1. Magnitude of DC Sources

Cascaded multilevel inverters are categorized as symmetric or asymmetric considering the value of the source/input voltages. Considering symmetric topology, value of all dc voltage sources is equivalent while magnitude of all dc voltage sources varies in asymmetric topologies. With equal number of basic units in the respective cascaded structures, asymmetric topologies produce higher levels of output voltage compared to symmetric topologies. Based on the above characteristics, symmetric and asymmetric computation of the dc sources is provided next subsection.

2.1.1. Symmetric DC Sources

Considering Figure 2, if the magnitude of input voltages is equal (symmetric characteristic) then 3-levels and 5-levels of output voltages are generated by Figure 2a and Figure 2b respectively. Let n represent the number of basic units in a given structure such as Figure 2a, therefore maximum/peak output voltage ($V_{o,n,\max}$) is expressed as:

For n = 2, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_{dc} \\ V_{o,2,\max} = V_1 + V_2 = 2V_{dc} \end{cases} \quad (3)$$

For n = 3, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_{dc} \\ V_{o,3,\max} = V_1 + V_2 + V_3 = 3V_{dc} \end{cases} \quad (4)$$

For n = 4, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_{dc} \\ V_{o,4,\max} = V_1 + V_2 + V_3 + V_4 = 4V_{dc} \end{cases} \quad (5)$$

For n = 5, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_5 = V_{dc} \\ V_{o,5,\max} = V_1 + V_2 + V_3 + V_4 + V_5 = 5V_{dc} \end{cases} \quad (6)$$

For n = 6, the maximum output voltage is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_5 = V_6 = V_{dc} \\ V_{o,6,\max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 6V_{dc} \end{cases} \quad (7)$$

Therefore, symmetric maximum/peak output voltage of the proposed MLI is expressed by:

$$V_{o,\max} = nV_{dc} \quad (8)$$

Similarly, the output voltage levels for symmetric dc sources of the proposed MLI Figure 2a is computed as:

For n = 2, the maximum output voltage level is computed by:

$$\begin{cases} V_1 = V_2 = V_{dc} \\ V_{o,2,\max} = V_1 + V_2 = 2V_{dc} \\ N_{LEVEL} = n + 1 = 3 - Levels \end{cases} \quad (9)$$

For n = 3, the maximum output voltage level is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_{dc} \\ V_{o,3,\max} = V_1 + V_2 + V_3 = 3V_{dc} \\ N_{LEVEL} = n + 1 = 4 - Levels \end{cases} \quad (10)$$

For n = 4, the maximum output voltage level is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_{dc} \\ V_{0,2,\max} = V_1 + V_2 + V_3 + V_4 = 4V_{dc} \\ N_{LEVEL} = n + 1 = 5 - Levels \end{cases} \quad (11)$$

For n = 5, the maximum output voltage level is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_5 = V_{dc} \\ V_{0,2,\max} = V_1 + V_2 + V_3 + V_4 + V_5 = 5V_{dc} \\ N_{LEVEL} = n + 1 = 6 - Levels \end{cases} \quad (12)$$

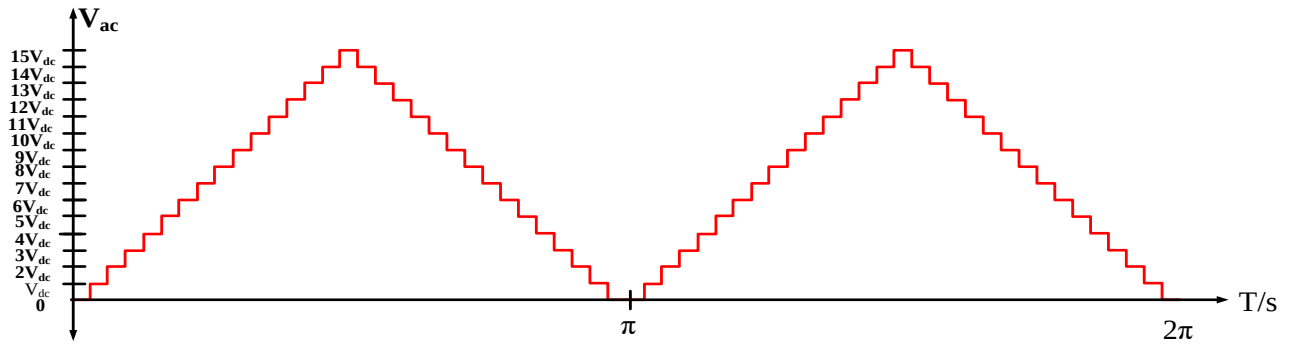


Figure 4. Positive 15-level waveform of proposed inverter

For n = 6, the maximum output voltage level is computed by:

$$\begin{cases} V_1 = V_2 = V_3 = V_4 = V_5 = V_6 = 1V_{dc} \\ V_{0,2,\max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 6V_{dc} \\ N_{LEVEL} = n + 1 = 7 - Levels \end{cases} \quad (13)$$

2.1.2. Asymmetric DC Sources

Asymmetric feature of the dc source implies a variation in the value of the dc sources. In asymmetric dc magnitude computation, binary or trinary computations are possible, the later produces more output levels compared to binary topologies.

Considering Figure 2, if the magnitude of input voltages is unequal (asymmetric characteristic) then 4-levels and 7-levels of output voltages are generated by Figure 2a and Figure 2b, respectively.

Let n represent the number of basic units in a given structure such as Figure 2a, therefore maximum or peak output voltage ($V_{o,n,\max}$) is expressed as:

For n = 2, the maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_{o,2,\max} = V_1 + V_2 = 3V_{dc} \end{cases} \quad (14)$$

For n = 3, the maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_{o,3,\max} = V_1 + V_2 + V_3 = 6V_{dc} \end{cases} \quad (15)$$

Again, for n = 3, maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_{o,3,\max} = V_1 + V_2 + V_3 = 7V_{dc} \end{cases} \quad (16)$$

For n = 4, the maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_{o,4,\max} = V_1 + V_2 + V_3 + V_4 = 8V_{dc} \end{cases} \quad (17)$$

Again, for n = 4, maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_{o,4,\max} = V_1 + V_2 + V_3 + V_4 = 15V_{dc} \end{cases} \quad (18)$$

For n = 5, the maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ V_{o,5,\max} = V_1 + V_2 + V_3 + V_4 + V_5 = 15V_{dc} \end{cases} \quad (19)$$

Again, for n = 5, maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ V_{o,5,\max} = V_1 + V_2 + V_3 + V_4 + V_5 = 31V_{dc} \end{cases} \quad (20)$$

For n = 6, the maximum output voltage for is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ V_6 = 6V_{dc} \\ V_{o,6,\max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 21V_{dc} \end{cases} \quad (21)$$

Again, for n = 6, maximum output voltage is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ V_6 = 32V_{dc} \\ V_{o,6,\max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 63V_{dc} \end{cases} \quad (22)$$

Similarly, the output voltage levels for asymmetric dc sources of the proposed MLI Figure 2a are expressed by:

For n = 2, the maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_{0,2,\max} = V_1 + V_2 = 2V_{dc} \\ N_{LEVEL} = 2n = 4 - Levels \end{cases} \quad (23)$$

For n = 3, maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_{0,3,\max} = V_1 + V_2 + V_3 = 6V_{dc} \\ N_{LEVEL} = 2n+1 = 7 - Levels \end{cases} \quad (24)$$

Again, for n = 3, the maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_{0,3,\max} = V_1 + V_2 + V_3 = 7V_{dc} \\ N_{LEVEL} = 2n+2 = 8 - Levels \end{cases} \quad (25)$$

For n = 4, maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_{0,4,\max} = V_1 + V_2 + V_3 + V_4 = 8V_{dc} \\ N_{LEVEL} = 2n+1 = 9 - Levels \end{cases} \quad (26)$$

Again, for n = 4, the maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_{0,4,\max} = V_1 + V_2 + V_3 + V_4 = 15V_{dc} \\ N_{LEVEL} = 2n+1 = 16 - Levels \end{cases} \quad (27)$$

For n = 5, maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ V_{0,5,\max} = V_1 + V_2 + V_3 + V_4 + V_5 = 15V_{dc} \\ N_{LEVEL} = 3n+1 = 16 - Levels \end{cases} \quad (28)$$

Again, for n = 5, the maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ V_{0,5,\max} = V_1 + V_2 + V_3 + V_4 + V_5 = 31V_{dc} \\ N_{LEVEL} = 6n+1 = 32 - Levels \end{cases} \quad (29)$$

For n = 6, maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 3V_{dc} \\ V_4 = 4V_{dc} \\ V_5 = 5V_{dc} \\ V_6 = 6V_{dc} \\ V_{0,6,\max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 21V_{dc} \\ N_{LEVEL} = 3n+4 = 22 - Levels \end{cases} \quad (30)$$

For n = 6, maximum output voltage level is computed as:

$$\begin{cases} V_1 = 1V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = 4V_{dc} \\ V_4 = 8V_{dc} \\ V_5 = 16V_{dc} \\ V_6 = 32V_{dc} \\ V_{0,6,\max} = V_1 + V_2 + V_3 + V_4 + V_5 + V_6 = 63V_{dc} \\ N_{LEVEL} = 10n+4 = 64 - Levels \end{cases} \quad (31)$$

From the above asymmetric and symmetric analysis of the magnitude of the dc sources, it's evident that asymmetric topologies generate higher levels of output voltage than symmetric topologies. Therefore, utilizing asymmetric dc sources in the proposed single-phase topology will result in an inverter composed of less power switches, less dc sources, reduced inverter size and volume. The proposed multilevel inverter of Figure 3a comprises eight semiconductor switches and four dc voltages. The switching sequences is shown in Table 1, the voltage values are equivalent to that of Equation (27). In the explanation below, only positive output voltage generation is given.

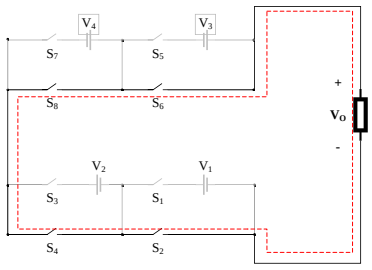
Maximum positive voltage of $15V_{dc}$ is generated during the 15th state where switches S_1, S_3, S_5, S_7 conducts while the remaining switches are in the voltage blocking mode. Output voltage of the 14th state is positive $14V_{dc}$ and in this state S_2, S_3, S_5, S_7 are active while the remaining are inactive. In the 13th state, the conducting switches are S_1, S_4, S_5, S_7 while the remaining switches are non-conducting and this generates positive $13V_{dc}$. In 12th state, positive $12V_{dc}$ is generated by conducting switches S_2, S_4, S_5, S_7, the rest of the switches are in voltage blocking mode. During the 11th state, the active switches are S_1, S_3, S_6, S_7 generating positive $11V_{dc}$.

Table 1. Switching Pattern

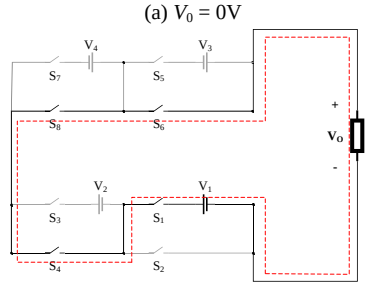
State	Switches	DC Sources	Output Voltage
1	S_1, S_4, S_6 and S_8	V_1	$1V_{dc}$
2	S_2, S_3, S_6 and S_8	V_2	$2V_{dc}$
3	S_1, S_3, S_6 and S_8	$V_1 + V_2$	$3V_{dc}$
4	S_2, S_4, S_5 and S_8	V_3	$4V_{dc}$
5	S_1, S_4, S_5 and S_8	$V_1 + V_3$	$5V_{dc}$
6	S_2, S_3, S_5 and S_8	$V_2 + V_3$	$6V_{dc}$
7	S_1, S_3, S_5 and S_8	$V_1 + V_2 + V_3$	$7V_{dc}$
8	S_2, S_4, S_6 and S_7	V_4	$8V_{dc}$
9	S_1, S_4, S_6 and S_7	$V_1 + V_4$	$9V_{dc}$
10	S_2, S_3, S_6 and S_7	$V_2 + V_4$	$10V_{dc}$
11	S_1, S_3, S_6 and S_7	$V_1 + V_2 + V_4$	$11V_{dc}$
12	S_2, S_4, S_5 and S_7	$V_3 + V_4$	$12V_{dc}$
13	S_1, S_4, S_5 and S_7	$V_1 + V_3 + V_4$	$13V_{dc}$
14	S_2, S_3, S_5 and S_7	$V_2 + V_3 + V_4$	$14V_{dc}$
15	S_1, S_3, S_5 and S_7	$V_1 + V_2 + V_3 + V_4$	$15V_{dc}$
16	S_2, S_4, S_6 and S_8	-	0

In the 10th state, the conducting switches which generate $10V_{dc}$ are S_2, S_3, S_6, S_7. In the 9th state, active switches which produce $9V_{dc}$ positive voltage are S_1, S_4, S_6, S_7. In the 8th state, conducting switches S_2, S_4, S_6, S_7 generate positive $8V_{dc}$. During the 7th state, positive $7V_{dc}$ voltage is generated by the following active switches; S_1, S_3, S_5, S_8. In the 6th state, $6V_{dc}$ is generated by the active switches S_2, S_3, S_5, S_8 while the remaining switches are in voltage blocking state. During the 5th state, active switches are S_1, S_4, S_5, S_8 generate $5V_{dc}$. In the 4th state, conducting switches are S_2, S_4, S_5, S_8 and the generated output voltage is $4V_{dc}$. During the 3rd state, the generated voltage is $3V_{dc}$ by the following conducting switches S_1, S_3, S_6, S_8. In the 2nd state, produced voltage is $2V_{dc}$ by the following conducting switches S_2, S_3, S_6, S_8 and finally the 1st state produces V_{dc} voltage when the following power switches S_1, S_4, S_6, S_8 are active.

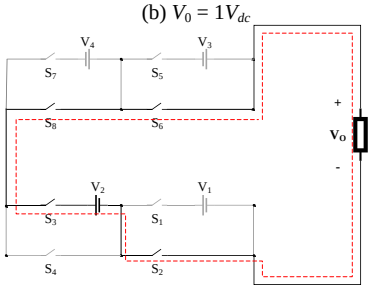
Zero voltage is generated when all switches connected to dc voltage sources are open i.e., S_2, S_4, S_6, S_8 are turned-on. These various states of switching are illustrated by Figure 5a to Figure 5p and Table 1 shows the switching pattern of the inverter for positive stepped output voltages.



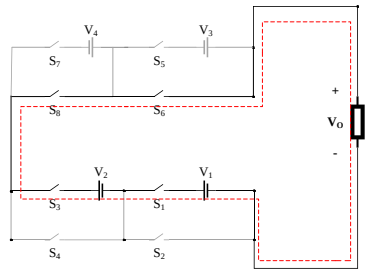
(a) $V_0 = 0V$



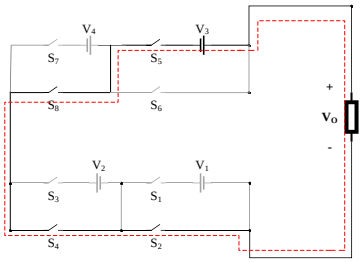
(b) $V_0 = 1V_{dc}$



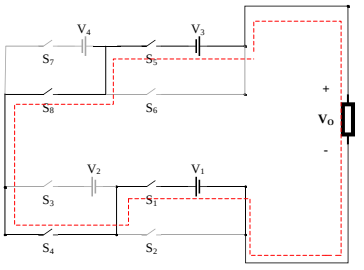
(c) $V_0 = 2V_{dc}$



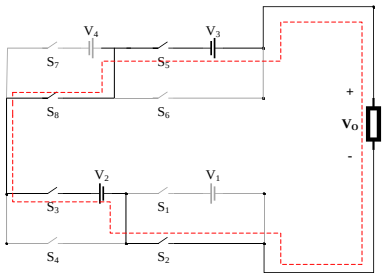
(d) $V_0 = 3V_{dc}$



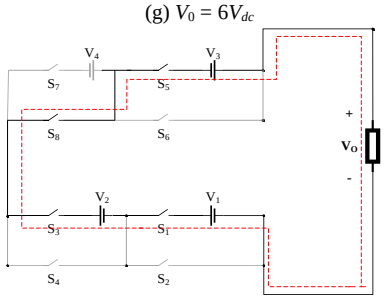
(e) $V_0 = 4V_{dc}$



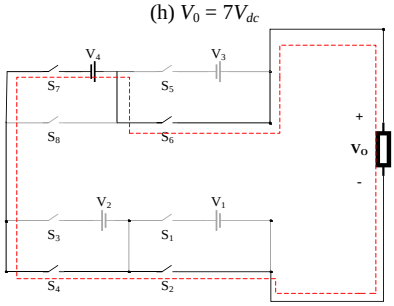
(f) $V_0 = 5V_{dc}$



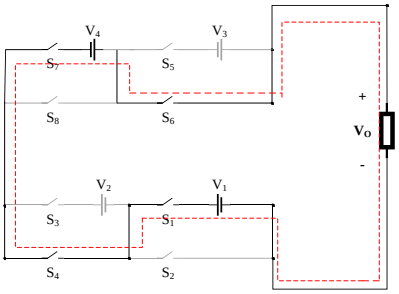
(g) $V_0 = 6V_{dc}$



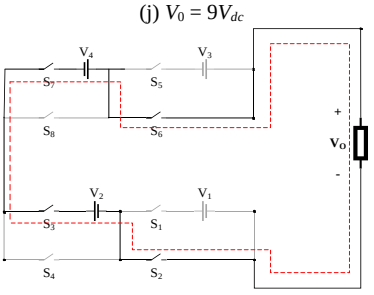
(h) $V_0 = 7V_{dc}$



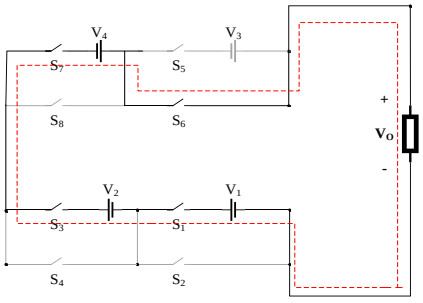
(i) $V_0 = 8V_{dc}$



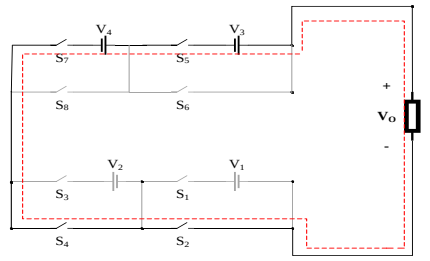
(j) $V_0 = 9V_{dc}$



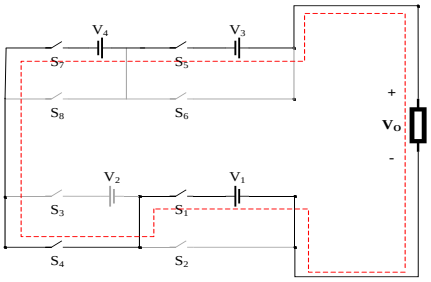
(k) $V_0 = 10V_{dc}$



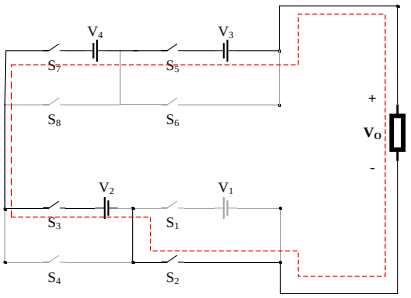
(l) $V_0 = 11V_{dc}$



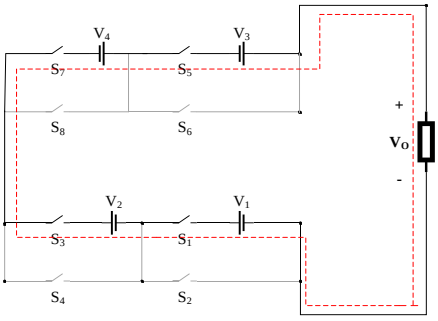
(m) $V_0 = 12V_{dc}$



(n) $V_0 = 13V_{dc}$



(o) $V_0 = 14V_{dc}$



(p) $V_0 = 15V_{dc}$

Figure 5. Switching states of proposed positive 16-level inverter

3. PROPOSED CASCADED 31-LEVEL MLI

Figure 6 shows the power circuit of the proposed cascaded 31-level single phase asymmetrical MLI. The proposed asymmetrical MLI is derived by cascading two submultilevel units of Figure 2a. Incorporating an H-bridge structure will enable the generation of positive and negative step output voltages. The component count for the proposed 31-level inverter are four dc sources, twelve unidirectional switches and twelve driver circuits.

The output voltage level count and component quantities are computed by Equation (32). Where $Q_{V_{dc}}$ is the dc source count, Q_{S_W} and Q_{D_R} represent the quantity of switches and driver circuit accordingly. Q_{LEVEL} and $V_{O_{MAX}}$ are the output voltage level and maximum output voltage, respectively.

$$\begin{cases} Q_{V_{dc}} = 4 \\ Q_{S_W} = Q_{D_R} = 12 \\ Q_{LEVEL} = 31 \\ V_{O_{MAX}} = 15V_{dc} \end{cases} \quad (32)$$

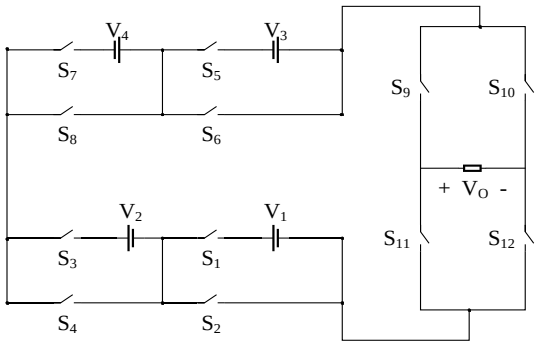


Figure 6. Proposed cascaded 31-level MLI inverter

3.1. Computation of Power Losses

Power losses of converters are determined by evaluating the following parameters. Conduction power losses, switching and standing voltage power losses. However, the standing voltage power losses are negligible but useful in converter cost determination.

3.1.1. Switching Power Losses

Switching power losses of converters are determined during the switching period of switch-on (turn-on) and switch-off (turn-off) of individual switches. For the proposed MLI, the switching power losses are computed as energy losses. Therefore, energy losses during the stage of switch-on and switch-off are given by E_{on} and E_{off} respectively. Let P_{SW} represent total switching losses. From Equation (33), the off-state switch voltage is given by V_{sw}. Also, the switch current during the period of switch-on and switch-off are expressed by I and I' respectively. Finally, switch-on time and switch-off time are expressed by t_{on} and t_{off} respectively. Solving Equations (33) and (34) will yield final P_{SW} Equation (35).

$$\begin{cases} E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt \\ E_{on,k} = \int_0^{t_{on}} \left[\left(\frac{I'}{t_{on}} t \right) \left(-\frac{V_{sw,k}}{t_{on}} (t - t_{on}) \right) \right] dt \\ E_{on,k} = \frac{1}{6} V_{sw,k} I' t_{on} \end{cases} \quad (33)$$

$$\begin{cases} E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt \\ E_{off,k} = \int_0^{t_{off}} \left[\left(\frac{V_{sw,k}}{t_{off}} \right) \left(-\frac{I}{t_{off}} (t - t_{off}) \right) \right] dt \\ E_{off,k} = \frac{1}{6} V_{sw,k} I t_{off} \end{cases} \quad (34)$$

$$P_{SW} = f_s \sum_{k=1}^{N_{switch}} \left(\sum_{i-1}^{N_{on,\,k}} E_{on,\,k} + \sum_{i=1}^{N_{off,\,k}} E_{off,\,k} \right) \quad (35)$$

3.1.2. Conduction Power Losses

Conduction power losses of a converter occurs when the power switches are conducting. The applied semiconductor switches of the proposed multilevel inverter are unidirectional switches with respect to the voltage and each switch is composed of one diode which antiparallel connected to an IGBT. Therefore, the conduction power losses of the diode and IGBT are computed separately and summed-up to give the conduction power losses of the converter. Let $P_{C,T}$ and $P_{C,D}$ represent IGBT conduction power losses and diode conduction power losses accordingly. The value of β is dependent on the type of semiconductor switch employed and it's a constant value provided by the manufacturer. From Equation (36), the resistance of the IGBTs and diodes are expressed by R_T and R_D respectively. Also, the IGBT voltage and diode voltage are expressed by V_T and V_D accordingly. Solving Equations (36) and (37) will yield the final P_C in Equation (38). The overall inverter losses and efficiency are computed by Equations (39) and (40) accordingly.

$$\begin{cases} P_{C,T}(t) = (V_T + R_T i^{\beta}(t))i(t) \\ P_{C,T} = \dfrac{1}{2\pi} \displaystyle\int_0^{2\pi} n_T(t)[V_T + R_T i^{\beta}(t))i(t)]d(\omega t) \end{cases} \quad (36)$$

$$\begin{cases} P_{C,D}(t) = (V_D + R_D i(t))i(t) \\ P_{C,D} = \dfrac{1}{2\pi} \displaystyle\int_0^{2\pi} n_D(t)[(V_T + R_D i(t))i(t)]d(\omega t) \end{cases} \quad (37)$$

$$P_C = P_{C,T} + P_{C,D} \quad (38)$$

Therefore, absolute power loss P_{Loss} of the inverter is computed by:

$$P_{Loss} = P_{sw} + P_C \quad (39)$$

Efficiency η of the inverter computed by:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{Loss}}{P_{in}} \quad (40)$$

3.2. Blocking Voltage

Blocking or standing voltage of a power electronic converter is determined by computing the off-state maximum voltage of individual power switches then summing them to give the total standing voltage of the converter. Standing voltage has a direct relationship with the cost of a converter. The higher the standing voltage, the higher the cost of converter. Similarly, the converter cost is reduced if the standing voltage is less. The proposed multilevel inverter of Figure 6 has 12 unidirectional power switches; 8 in the main circuit and 4 in the H-bridge. Hence, the standing voltage ($V_{Standing}$) of the proffered multilevel inverter is determined by:

$$V_{Standing} = \sum_{k=1}^{s} \sum_{j=1}^{j} V_{s,k,j} \quad (41)$$

where, $V_{s,k,j}$ is the blocking voltage of unidirectional switches $S_{k,1}$, $S_{k,2}$ … $S_{k,12}$ for the kth switch. The blocking voltage of the 8 main circuit switches are expressed by:

$$V_{S_1} = V_{S_2} = 1V_{dc} \quad (42)$$

$$V_{S_3} = V_{S_4} = 2V_{dc} \quad (43)$$

$$V_{S_5} = V_{S_6} = 4V_{dc} \quad (44)$$

$$V_{S_7} = V_{S_8} = 8V_{dc} \quad (45)$$

The blocking voltage of the 4 H-bridge switches are expressed by:

$$V_{S_9} = V_{S_{10}} = V_{S_{11}} = V_{S_{12}} = 15V_{dc} \quad (46)$$

Hence, the absolute standing voltage of the converter is computed as:

$$V_{Standing} = 2(15V_{dc}) + 4(15V_{dc}) = 90V_{dc} \quad (47)$$

$$V_{Standing} = 90V_{dc} = 90(15\text{V}) = 1350\ \text{V} \quad (48)$$

4. FUNDAMENTAL FREQUENCY CONTROL

Nearest level control (NLC) also known as fundamental frequency control (FFC) is employed in switching the proposed single-phase multilevel inverter. Figure 7 shows the concept of NLC operations in producing 7-levels of output voltage. To generate each voltage level, the reference voltage is compared to the step voltage, the intersecting point determines the voltage level to be selected. If this point is closer to upper voltage level, then that magnitude of output voltage is generated. However, if the point is closer to the lower voltage level, then that magnitude of voltage is generated. Basically, NLC enables selection of closest (nearest) voltage level to be generated by the proposed MLI. For three-phase inverter control, each phase is controlled independently with phase difference of 120°. NLC technique is much simplified with respect to its algorithm when compared to NVC (nearest vector control) because selecting the closest value is simple. In three-phase inverter control, NLC provides independent phase controls unlike SVC which controls three-phase inverters directly.

5. COMPARATIVE ANALYSIS

The proposed 31-level single-phase MLI is juxtaposed with other multilevel inverter topologies with respect to output voltage levels, dc voltages, switch as well as driver circuits and total component count. This comparative analysis, illustrated in Table 2 enables us to showcase the merits and demerits of the proposed MLI. All referenced topologies in Table 2 generate 31-levels of output voltage. Considering quantity of switches (IGBT), the proposed topology and reference [22] require the least quantity of switches, reference [20] utilizes the highest quantity of switches and driver circuits. Considering the quantity of dc sources required, the proposed topology utilizes 4 dc sources which is equivalent to the dc source required by references [17] and [19]. References [18] and [22] used 3 dc sources respectively. Also, references [20] and [21] used 2 dc sources, respectively.

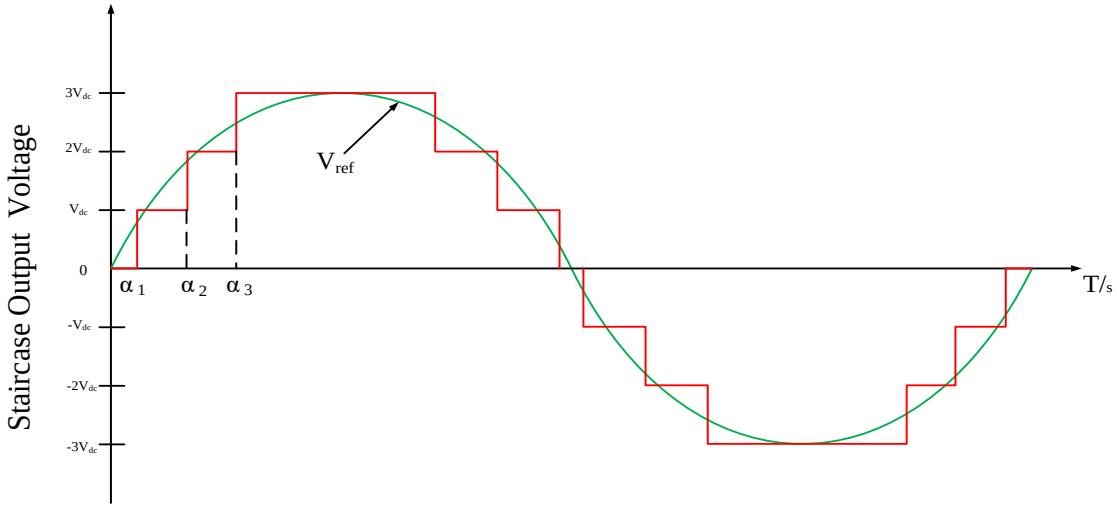


Figure 7. NLC technique

Table 2. Comparative Analysis

Topology	[17]	[18]	[19]	[20]	[21]	[22]	[23]	Proposed
Output Level, N_L	31	31	31	31	31	31	31	31
Switches, N_{IGBT}	16	14	14	18	16	12	14	12
Driver Circuit, N_{DR}	12	12	14	18	16	12	10	12
DC Source, N_{DC}	4	3	4	2	2	3	6	4
Capacitors, N_C	-	-	-	4	4	4	-	-
Diodes, N_D	-	-	-	2	2	-	-	-
Total Components	32	29	32	44	40	31	30	28

However, they also used 4 capacitors each. Reference [22] used 3 dc sources and 4 capacitors. Reference [23] used the highest number of 6 dc sources. The proposed 31-level multilevel inverter does not utilize extra diodes or capacitors. But, references [20], [21] and [22] used diodes and capacitors. With respect to the number of driver circuit required, the proposed topology together with other topologies require less numbers, however, the topology in [23] requires the barest minimum quantity of driver circuits. Considering total components needed, proffered topology needs the barest minimum component count.

6. SIMULATION RESULTS

This section provides simulation studies for the proposed cascaded single-phase 31-level inverter illustrated by Figure 6. The cascaded structure is made-up of two submultilevel units having 4 dc sources, 12 power switches and *RL* load. Simulation of the proposed inverter was done by building its power circuit in PSCAD/EMTDC software. Table 3 shows the simulation parameters. Figures 8 to 10 shows output waveforms of the proffered cascaded multilevel inverter.

Table 3. Simulation Parameters

Parameters	Magnitude
Switching Frequency, f_s	50 kHz
Load frequency, f_o	50 Hz
DC Sources, V_{dc}	$V_1 = 15V$, $V_2 = 30V$ $V_3 = 60V$, $V_4 = 120V$
Modulation Index	1
Load Resistance, R	50 Ω
Load Inductance L	0.055 H

The load voltage and reference voltage waveforms are shown by Figure 8. As depicted by the waveforms, the step load voltage waveform is perfectly superimposed on the reference sinusoidal waveform. The maximum load voltage is 225 V with a frequency of 50 Hz. Varying the magnitude of input voltages will vary the magnitude of the output voltage. Figure 9 shows the load current waveform with a peak value of 4.23 A. Figure 10 shows the standing voltage waveforms for every switch in the proffered 31-level inverter. The standing voltage across switch S_1 and S_2 is 15 V. The standing voltage across switch S_3 and S_4 is 30 V. The standing voltage across switch S_5 and S_6 is 60 V. The standing voltage across switch S_7 and S_8 is 120 V. All the switches in the H-bridge have equal standing voltages i.e., S_9, S_{10}, S_{11} and S_{12} have 225 V standing voltage across them. The load voltage and current waveforms contain less distortion i.e., they are perfect sinusoidal waveforms.

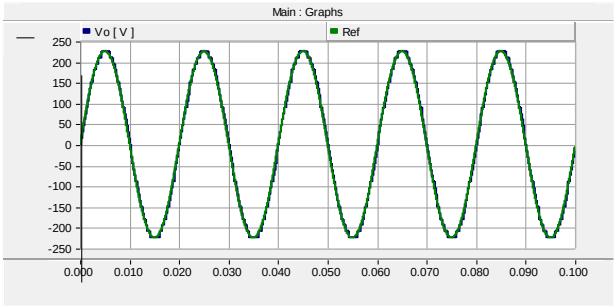


Figure 8. Load voltage and reference voltage waveforms

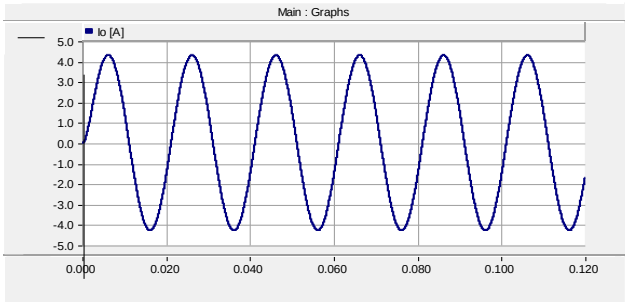
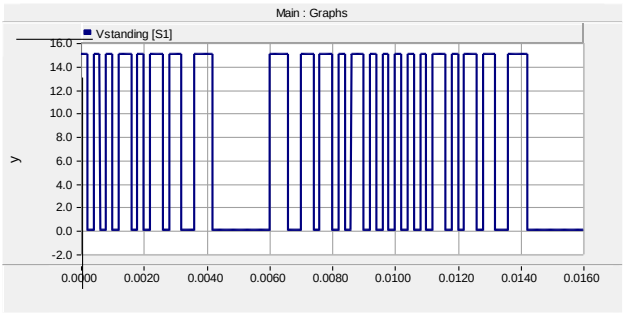
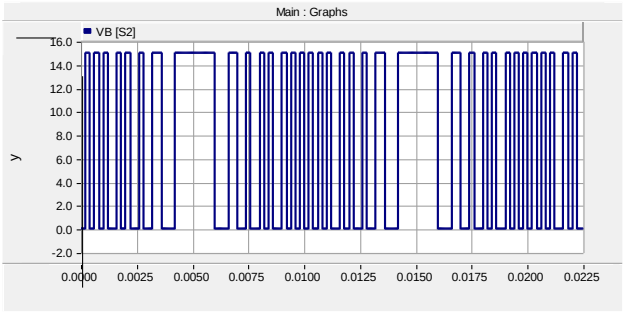


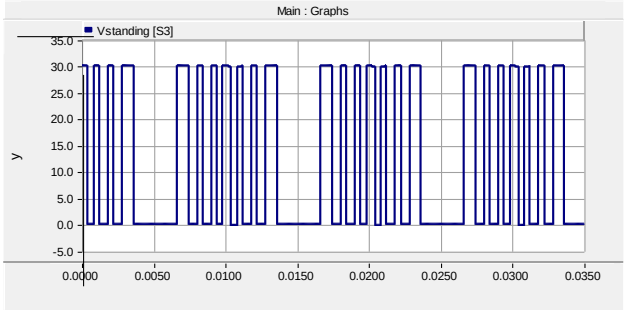
Figure 9. Load current waveform


Main : Graphs
Vstanding [S1]
y

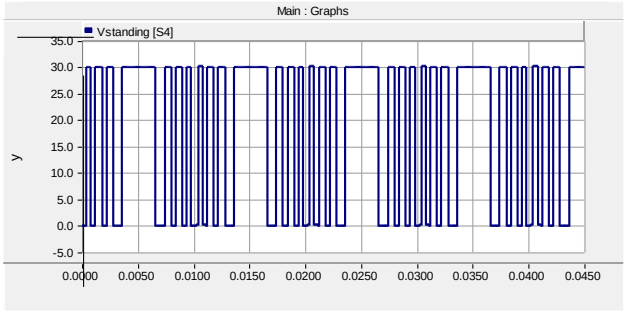
(a)


Main : Graphs
VB [S2]
y

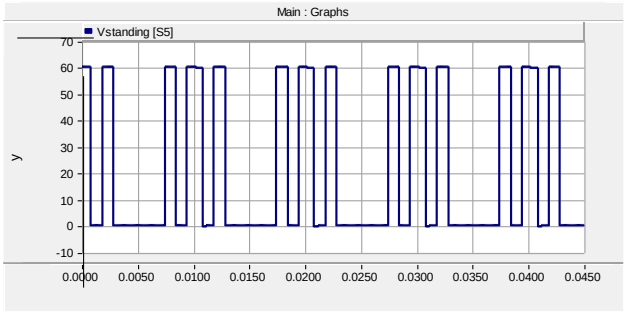
(b)


Main : Graphs
Vstanding [S3]
y

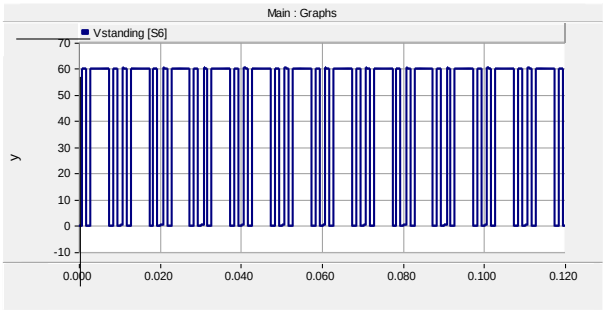
(c)


Main : Graphs
Vstanding [S4]
y

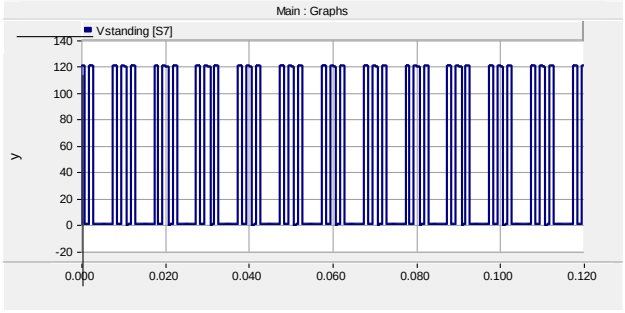
(d)


Main : Graphs
Vstanding [S5]
y

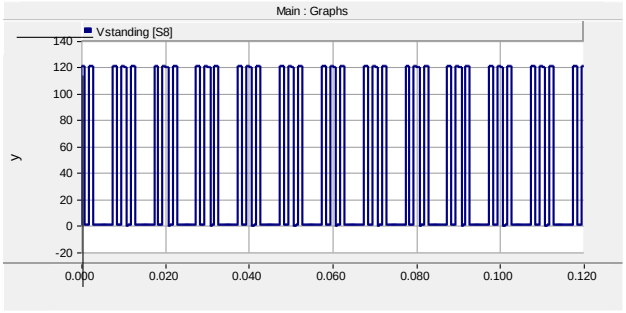
(e)


Main : Graphs
Vstanding [S6]
y

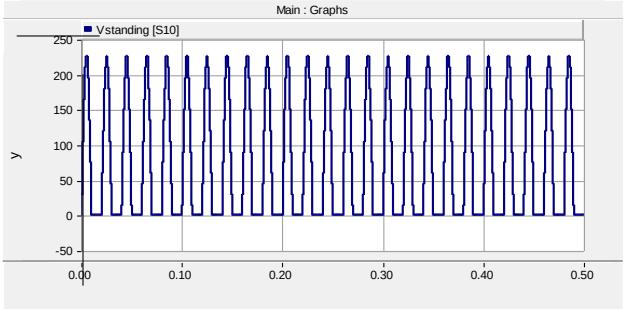
(f)


Main : Graphs
Vstanding [S7]
y

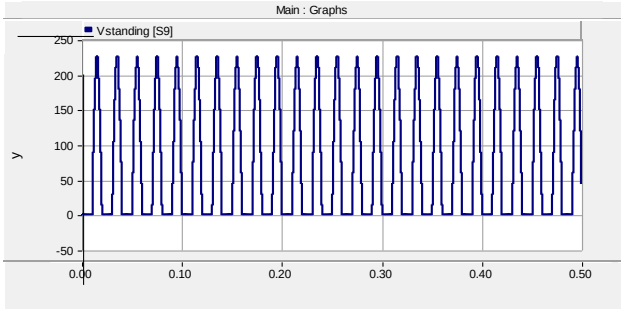
(g)


Main : Graphs
Vstanding [S8]
y

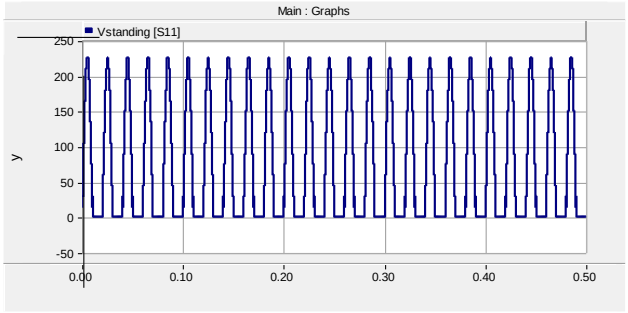
(h)


Main : Graphs
Vstanding [S10]
y

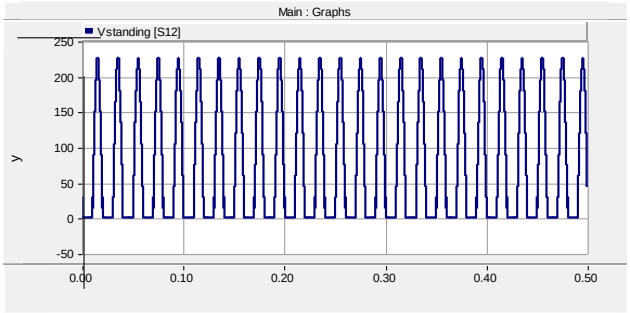
(i)


Main : Graphs
Vstanding [S9]
y

(j)



(k)



(l)

Figure 10. Standing voltage waveforms of switches

7. CONCLUSIONS

New cascaded multilevel inverter topologies based on basic and submultilevel units are introduced by this paper. The submultilevel units are derived by cascading two basic units. The proposed cascaded topologies generate only positive output voltages and thus require an H-bridge to generate negative output voltages. The peak load voltage and load voltage levels of the proffered multilevel inverter are examined under symmetric and asymmetric dc voltage characteristics. Among the proposed topologies is a cascaded 31-level single-phase inverter composed of two cascaded submultilevel units and an H-bridge. The components count are 12 unidirectional switches, 4 dc sources, 12 driver circuits and an *RL* load. Comparative evaluation of the proposed 31-level inverter and some published topologies show that the proposed MLI utilizes less quantities of components i.e., the quantity of dc voltage sources, IGBTs and driver circuits required are less. Also, comparing the proposed topology to cascaded H-bridge, flying capacitor and diode-clamped MLI shows that these conventional topologies require more dc sources, IGBTs, clamping diodes and flying capacitors. Also, higher levels of output voltage are not possible in diode-clamped and flying capacitor topologies because the power circuit becomes complex and difficult to control. The proposed 31-level inverter requires less components which means that, the size, volume and installation area minimized. Using lower rated switches is based on reducing the standing voltage which translates to reduced inverter cost. Also, lower rated switches have less dv/dt stress and therefore perform better. Theoretical power loss computation, standing voltage computation and simulation are provided. Simulation of proposed inverter was carried out by building its power circuit in PSCAD/ EMTDC software. The load voltage, current and standing voltage waveforms perfectly align with the theoretical waveforms.

REFERENCES

[1] B.P. McGrath, D.G. Holmes, "Natural Capacitor Voltage Balancing for a Flying Capacitor Converter Induction Motor Drive", IEEE Transactions on Power Electronics, Vol. 24, No. 6, pp. 1554-1561, June 2009.

[2] S.N. Tackie, E. Babaei, "Modified Topology for Three-Phase Multilevel Inverters Based on a Developed H-Bridge Inverter", Electronics, Vol. 9, No. 11, pp. 2-17, 2020.

[3] M. di Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, P.J. Grbovic, "Five-Level E-Type Inverter for Grid-Connected Applications", IEEE Transactions on Industry Applications, Vol. 54, No. 5, pp. 5536-5548, September 2018.

[4] K. Wang, Z. Zheng, D. Wei, B. Fan, Y. Li, "Topology and Capacitor Voltage Balancing Control of a Symmetrical Hybrid Nine-Level Inverter for High-Speed Motor Drives", IEEE Trans. Ind. Appl., Vol. 53, No. 6, pp. 5563-5572, December 2017.

[5] F.P. Feletto, R.A. Durham, E.D.C. Bortoni, J.G. de Carvalho Costa, "Improvement of MV Cascaded H-Bridge Inverter (CHBI) VFD Availability for High-Power ESP oil Wells", IEEE Trans. Ind. Appl., Vol. 55, No. 1, pp. 1006-1011, February 2019.

[6] M.S. Bendyk, P.C. Luk, M.H. Alkhafaji, "Control Strategy for a Modified Cascaded Multilevel Inverter with Dual DC Source for Enhanced Drive Train Operation", IEEE Trans. Ind. Appl., Vol. 53, No. 5, pp. 4655-4664, September 2017.

[7] B. Singh, P. Kant, "Multipulse AC-DC Converter Fed 15-Level Cascaded MLI-Based IVCIMD for Medium-Power Application", IEEE Trans. Ind. Appl., Vol. 55, No. 1, pp. 858-868, February 2019.

[8] A. Lesnicar, R. Marquardt, "An Innovative Modular Multilevel Converter Topology Suitable for a Wide 324 Power Range", Proc. IEEE Power Tech. Conf., Vol. 3, Bologna, Italy, 2003.

[9] H.S. Patel, R.G. Hoft, "Generalized Techniques of Harmonic Elimination", IEEE Trans. Ind. Applicat., Vol. IA-9, pp. 310-317, 1973.

[10] M.A. Hosseinzadeh, M. Sarebanzadeh, M. Rivera, E. Babaei, P. Wheeler, "A Reduced Single-Phase Switched-Diode Cascaded Multilevel Inverter", IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 9, No. 3, pp. 3556-3569, June 2021.

[11] M. Vijeh, et al., "A General Review of Multilevel Inverters Based on Main Sub-Modules: Structural Point of View", IEEE Trans. Power Electron, Vol. 34, No. 10, pp. 9479-9502, October 2019.

[12] S. Sabyasachi, V.B. Borghate, R.R. Karasani, S.K. Maddugari, H.M. Suryawanshi, "A Fundamental Frequency Hybrid Control Technique Based Three Phase Cascaded Multilevel Inverter Topology", IEEE Access, Vol. 5, pp. 26912-26921, 2017.

[14] M.F. Kangarlu, E. Babaei, "A Generalized Cascaded Multilevel Inverter using Series Connection of Submultilevel Inverters", IEEE Transactions on Power Electronics, Vol. 28, No. 2, pp. 625-636, 2013.

[15] S.N. Tackie, B.K. Kurehwatira "Switched Inductor Capacitor Based DC-AC Converter for PV Applications",

International Journal on Technical and Physical Problems of Engineering (IJTPE), Issue, Vol. 14, No. 1, pp. 238-246, March 2022.
[16] A.R. Dash, A.K. Panda, R. Patel, T. Penthia, "Design and Implementation of a Cascaded Transformer Coupled Multilevel Inverter-based Shunt Active Filter under Different Grid Voltage Conditions", International Transactions on Electrical Energy Systems, Vol. 29, No. 2, pp. 27-28, 2019.
[17] S. Hussain, K.K. Qureshi, J. Gu, M.U. Asad, N. Butt, U. Farooq, "A New Topology with 31-Levels for Cascaded Multilevel Inverters", International Conference on Electromechanical and Energy Systems (SIELMEN), pp. 393-397, 2021.
[18] C. Dhanamjayulu, P. Kaliannan, S. Padmanaban, P. K. Maroti, J.B. Holm Nielsen, "A New Three-Phase Multi-Level Asymmetrical Inverter with Optimum Hardware Components", IEEE Access, Vol. 8, pp. 212515-212528, 2020.
[19] D. Prasad, C. Dhanamjayulu, S. Padmanaban, J.B. Holm Nielsen, F. Blaabjerg, S.R. Khasim, "Design and Implementation of 31-Level Asymmetrical Inverter with Reduced Components", IEEE Access, Vol. 9, pp. 22788-22803, 2021.
[20] A. Ahmad, M. Anas, A. Sarwar, M. Zaid, M. Tariq, J. Ahmad, A.R. Beig, "Realization of a Generalized Switched Capacitor Multilevel Inverter Topology with Less Switch Requirement", Energies, Vol. 13, Issue 7, March 2020.
[21] T. Roy, P.K. Sadhu, A. Dasgupta, "Cross-Switched Multilevel Inverter Using Novel Switched Capacitor Converters", IEEE Transactions on Industrial Electronics, Vol. 66, No. 11, pp. 8521-8532, November 2019.
[22] M.R. Hussan, A. Sarwar, M.D. Siddique, S. Mekhilef, S. Ahmad, M. Sharaf, M. Zaindin, M. Firdausi, "A Novel Switched-Capacitor Multilevel Inverter Topology for Energy Storage and Smart Grid Applications", Electronics, Vol. 9, Issue 10, October 2020.
[23] R.S. Alishah, S.H. Hosseini, E. Babaei, M. Sabahi, "Optimal Design of New Cascaded Switch-Ladder Multilevel Inverter Structure", IEEE Transactions on Industrial Electronics, Vol. 64, No. 3, pp. 2072-2080, March 2017.

BIOGRAPHIES

Name: **Samuel**
Middle Name: **Nii**
Surname: **Tackie**
Birthday: 27.03.1988
Birth Place: Accra, Ghana
Bachelor: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Faculty of Engineering, Ho Technical University, Ho, Ghana, 2007
Master: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2015
Doctorate: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2021
The Last Scientific Position: Assist. Prof., Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2021
Research Interests: Power Electronics, Renewable Energy Sources, Power Quality
Scientific Publications: 10 Papers
Scientific Memberships: IEEE

Name: **Nenubari**
Middle Name: **Marvin**
Surname: **Komi**
Birthday: 24.08.1994
Birth Place: Bori, Nigeria
Bachelor: Electrical Engineering, Department of Electrical and Electronic Engineering, Faculty of Engineering, Rivers State University, Port Harcourt, Nigeria, 2018
Master: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2022
Research Interests: Power Electronics, Renewable Energy Sources
Scientific Memberships: NSE (Nigerian Society of Engineers)

Name: **Ozgur**
Middle Name: **Cemal**
Surname: **Ozerdem**
Birthday: 11.11.1967
Birth Place: Ankara, Turkey
Bachelor: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Faculty of Engineering, Eastern Mediterranean University, Famagusta, Northern Cyprus, 1992
Master: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Faculty of Engineering, Eastern Mediterranean University, Famagusta, Northern Cyprus, 1994
Doctorate: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2005
The Last Scientific Position: Prof., Department of Electrical and Electronic Engineering, Engineering Faculty, European University of Lefke, Lefke, Northern Cyprus, 2022
Research Interests: Power Systems, Power Electronics, Renewable Energy Sources, Power quality
Scientific Publications: 40 Papers
Scientific Memberships: IEEE Senior Member