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LOGIC GATES BASED ON THERMAL MEMORY ELEMENTS

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Abstract- This study proposes models of AND and OR logic gates based on a thermal memory element. Models were built using the SolidWorks software package. Simulation modeling of the work of such elements is carried out on the ANSYS Workbench platform using the transient thermal module for non-stationary thermal calculations. This made it possible to estimate the power of the heat flows arising at the inputs of the logic gate because of heating by 2 ℃. For the design under consideration, during the virtual experiment equal to 1 s, the power of the heat flux after 0.01 s was 7e+5 pW/μm^2, which is sufficient to transfer heat to the output of the logic gate. The required voltage of 2.5 V for heating and setting the output value is comparable to the same parameter for memristors based on $CaTiO_3$ perovskites, a rare earth element. The thermal memory elements used are based on the Al-Si-SiO_2 structure, which is more cost-effective and suitable for integration with current ICs. This article provides a table comparing different types of analog memory. The purpose of this study is to demonstrate the possibility of using the thermal memory element design we developed to create logic gates as part of global research aimed at developing the architecture of in-memory computing. Thermal analogues of logic gates open the way to the implementation of thermal interaction circuits in artificial neural networks.

Keywords: Logic Gate, Analog Memory, Thermal Memory Element, Memristor, Memory Computation, Thermal Field Propagation.

1. INTRODUCTION

The basic elements of logic circuits form the computing core of computers [1]. We are working on thermal elements of logic circuits to perform logic procedures similar to the functioning of electronic logic nodes. A logical node in electronics is an element that performs a logical calculation on the data supplied to the input, based on a current pulse with separate discrete levels [2]. Thermal logic elements rely on non-additive heat transfer in a combination of analog (thermal) memory elements because of the temperature-dependent power spectrum. In this paper, we consider the application of thermal memory elements, which we introduced in [3-5], as logic gates in dielectric pocket designs. The operation of the thermal memory element is based on a continuous linear change in the temperature of the memory material during the SET and RESET processes [3], i.e., properties similar to those of memristive devices.

The similarity in the operation of these analog memory elements discovered by the authors allowed us to propose the use of thermal memory elements for implementing logic gates. Our memory element is a volatile unit, but unlike analogs, the ability to increase the heating temperature to 300 degrees provides a sufficient number of programmable states to create various combinations of logic gates. The variability of the device, which appears due to the thermodynamic influence of elements on each other, is accepted to be leveled with the help of a layer of dielectric thermal insulation. Let us consider the logic of operation of the thermal memory element and present a geometric model of the device obtained because of the formation of a thermal insulation dielectric layer. At the end of the article, we present the results of calculating a three-dimensional model of the designed logic elements and compare the characteristics of different types of memory elements

2. LITERATURE REVIEW

Resistive analog memory elements, so-called memristors, have gained popularity in recent years [6-15]. These elements are realized on materials with phase transitions under the influence of electric, magnetic, and thermal fields. Such materials include chalcogenides, ferroelectrics (polar dielectrics), and some types of dielectrics in which phase transition occurs under the influence of high temperatures. In [6], Julien Borgetti, et al. demonstrated that a logical NAND procedure can be implemented on three resistive memory elements connected to a load resistor, which implies the development of the entire Boolean algebra of logic. It was later presented that a similar logic circuit could be designed in a resistive memory chip with two elements on the same bit line, but in different word lines [7].

Several interconnect architectures based on NOR resistive memory elements were demonstrated [8-10]. Other extensions of the physics of resistive memory devices to in-memory logic algebra procedures include the modification of complex structures demonstrated by ferroelectric domain switching [11], the physics of crystallization [12] and melting [13] of phase change

materials. The ability of materials to preserve a phase transition was used to calculate the main arithmetic processes of addition, multiplication, division and subtraction with simultaneous storage of the result [14].

However, the limited number of non-volatile conduction (non-volatile conductivity state is one in which a semiconductor has the properties of a conductor, regardless of the supply voltage) states offered by modern memristors is an obstacle to their use in memristor computing. Moreover, the inability to accurately reproduce the degree of conductivity suggests the presence of defective and energy dependent devices [15]. Therefore, further research and discussions on new physical models of computation are required to develop a computing device based on interacting memristor elements to solve complex computational problems.

3. PROPOSED APPROACH (METHODS)

3.1. Thermal Memory Element

The thermal memory element is based on the technical task of simplifying the design of the memory element in contrast to the analogues described above. The Al-Si-SiO_2 structure used contains an Al-Si metallization system manufactured using vacuum deposition by electron beam metal evaporation. The operation logic of the thermal memory element is based on the dynamic temperature change of the conductive track of aluminum (Al) deposited on silicon (Si). Heat dissipation occurs mainly through contact with the silicon wafer. The thermal field propagates not only deep into the silicon wafer but also across its width around the heat source. To solve the boundary value problem of nonstationary heat conduction, mathematical modeling methods were used to simplify the general mathematical formulation. Taking into account the small volume of the aluminum film V_{Al} = 9e+5 μm^3 (Figure 2) compared with the volume of the substrate V_{Si} = 6e+8 μm^3, it was assumed that heating throughout the entire volume of the film occurs instantly. The applied heat flow powers do not change the thermal diffusivity coefficient. A diagram of the solution region is shown in Figure 1.

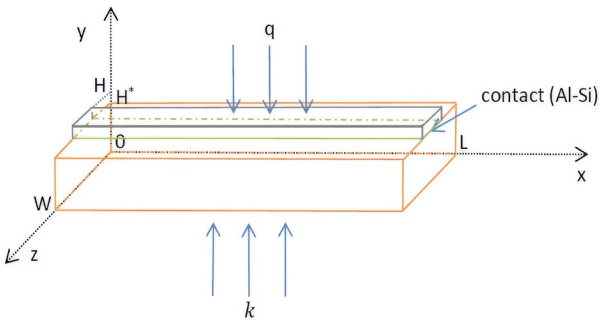

Figure 1. Diagram of the solution area (original authors' design)

In the first stage, the temperature distribution over the thickness of the plate was calculated using the finite difference method to solve the linear problem of thermal conductivity during the surface heat transfer of materials with different physical parameters.

The mathematical formulation of the problem has the following form:

$$\begin{cases} \rho_1 c_1 \dfrac{\partial T_1}{\partial t} = \lambda_1 \dfrac{\partial^2 T_1}{\partial y^2}\ ,\ H < y < H^* \\ \rho_2 c_2 \dfrac{\partial T_2}{\partial t} = \lambda_2 \dfrac{\partial^2 T_2}{\partial y^2}\ ,\ H^* < y < 0 \end{cases} \tag{1}$$

The initial and boundary conditions are as follows:

$$t = 0:\ T = T(0)\ ,\ 0 < y < H$$

$$y = 0:\ \lambda \frac{\partial T}{\partial y} = k\left(T^e - T\right)\ ,\ t > 0$$

$$y = H:\ -\lambda \frac{\partial T}{\partial y} = q\ ,\ t > 0 \tag{2}$$

$$\begin{cases} T_1\left(t, H^*\right) = T_2\left(t, H^*\right) \\ -\lambda_1 \dfrac{\partial T_1}{\partial y}\bigg|_{y = H^*} = -\lambda_2 = \dfrac{\partial T_2}{\partial y}\bigg|_{y = H^*} \end{cases}$$

The second stage was to determine the distribution of temperature over the silicon surface from an instantly heated aluminum layer throughout the entire thickness, considering the geometry of the silicon wafer. We considered a quasi-three-dimensional model with convection along the third coordinate. The location of the convective heat transfer is indicated in Figure 1 with arrows and the heat transfer coefficient k. This type of heat transfer is considered in the case of several memory elements located under each other with an air gap.

We used the temperature distribution over the thickness of the silicon layer from the first stage of the solution. The heat equation is two-dimensional. The mathematical formulation of the problem has the following form:

$$\rho c \frac{\partial T}{\partial t} = \lambda \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} \right) + 2k \frac{\left(T^e - T\right)}{h} \Bigg|, \begin{matrix} L_x < x < L \\ L_x < y < H^* \end{matrix} \tag{3}$$

The initial and boundary conditions are as follows:

$$t = 0:\ T = T_0\ ,\ 0 \le x \le L_x\ ,\ 0 \le y \le H^*$$

$$x = L_x:\ T = T_{cont}\ ,\ t > 0$$

$$x = L:\ T = T^e\ ,\ t > 0 \tag{4}$$

$$y = L_x:\ \frac{\partial T}{\partial y} = 0\ ,\ t > 0$$

$$y = H^*:\ \frac{\partial T}{\partial y} = 0\ ,\ t > 0$$

The spread of temperature over the silicon surface influences neighboring memory elements and changes their thermodynamic state. To solve this problem, a method was proposed to create dielectric (SiO_2) insulation inside silicon in the form of pockets because of the EPIC process [16]. To investigate the influence of thermal insulation pockets on the thermal field propagation around the thermal memory element, modeling of the thermal memory elements isolated in this way was carried out on the ANSYS Workbach platform with calculations in the Steady-State Thermal module.

The geometrical model (1 in Figure 2) with thermal memory elements isolated from each other by dielectric (SiO_2 pockets is a silicon wafer of 2 mm height with inclusions of 4 dielectric layers (3 in Figure 2). Each dielectric layer is inserted 30 μm deep into the silicon wafer and has a thickness of 1 μm, which corresponds to the dimensions of the insulating silicon dioxide film obtained from the EPIC process [16]. The dimensions of the thermal cells correspond to the experimental data (2 in Figure 2) [3, 5]. The length of the insulating layer is equal to the length of the conductive track of the thermal cell and corresponds to 4 mm (Figure 2).

Because of the modeling, the regions of thermal field propagation are obtained, which show the limitation of thermal field propagation when an insulated pocket is placed in the silicon wafer. Temperature values at equidistant areas from the boundaries of isolated and non-isolated memory elements were. The calculations showed that when the distance from the boundary of the conductive track to the wall of the insulating pocket is reduced by 20 times, the depth of the thermal field propagation decreases by four times. The results of the calculations were saved as images (Figure 3).

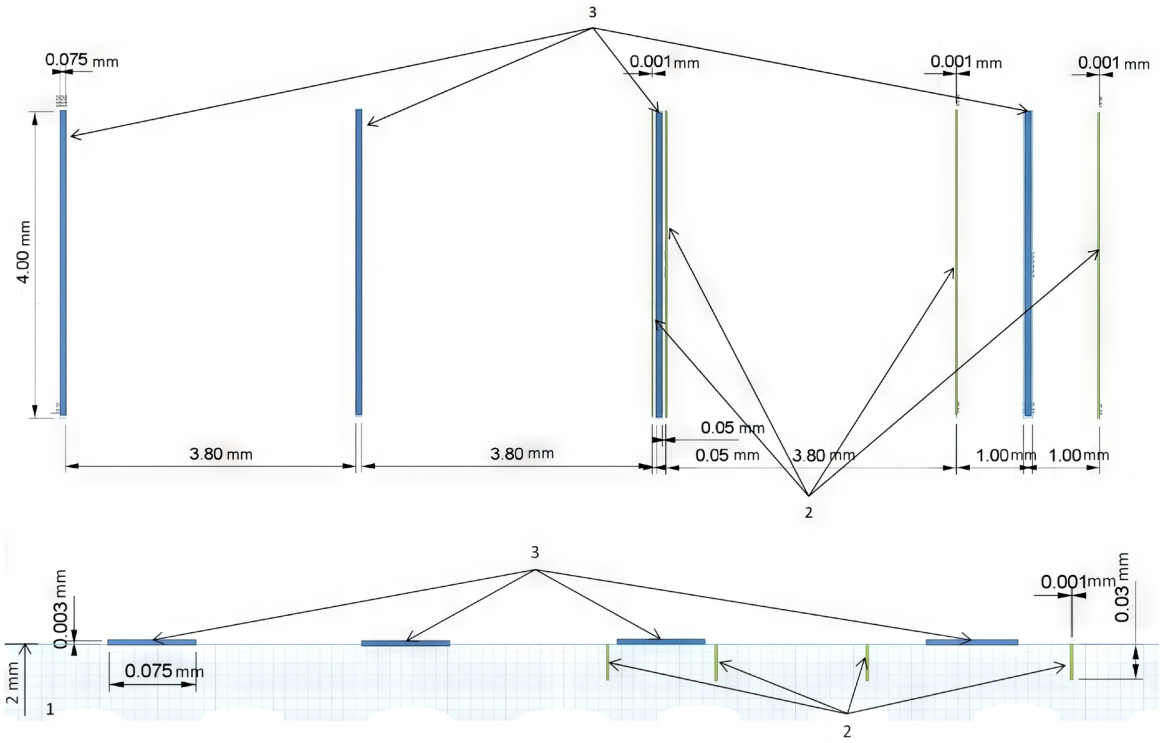

Figure 2. Geometry of the structure: 1- silicon wafer; 2- metal tracks for heating the structure; 3- dielectric layers (original authors' design)

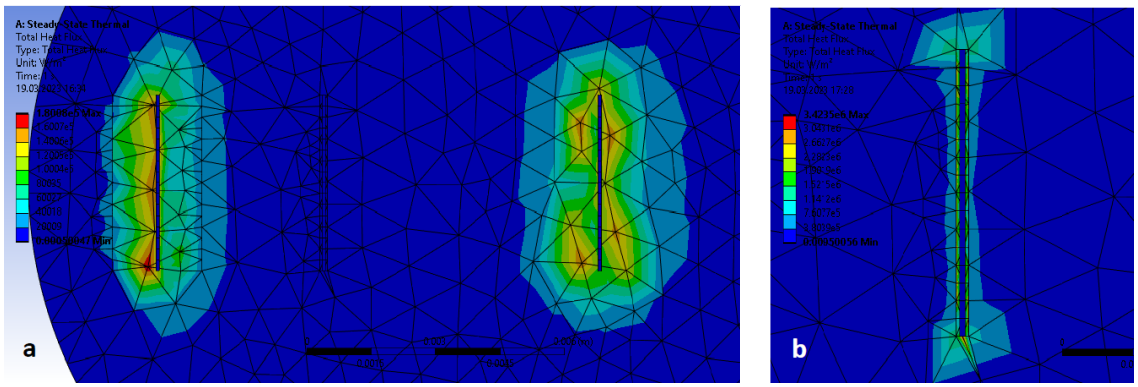

Figure 3. Thermal field propagation: a) around a cell in the boundary of a wide pocket and a cell without thermal insulation, b) around a cell in the boundary of a narrow pocket (original authors' design)

The presented calculations clearly show the possibility of controlling the propagation of the thermal field from a heated memory element in a silicon substrate through the inclusion of silicon dioxide layers. The use of a dielectric layer limiting the propagation of the thermal field made it possible to design circuits of two logic gates "AND" and "OR" on the basis of thermal memory elements. Simulation modeling of the operation of such elements was performed on the ANSYS Workbench platform using the Transient Thermal module for unsteady thermal calculations.

3.2. Logic gates AND and OR

The design of the structure (Figure 4) of the logic gates includes three thermal memory elements, two of which are used to store input data and one of which is designed to perform the calculation operation and save the result. The memory elements that receive the input data are arranged parallel to each other and separated by a dielectric layer to limit heat propagation and reduce the probability of changing each other's thermodynamic state. The third memory element, the logic gate output, is located under this dielectric layer. Figure 4 shows the geometry of the structure, which is bordered on three sides by the dielectric layer. The absence of a separating dielectric layer on the output side of the logic gate allows its connection to other logic gates to be realized.

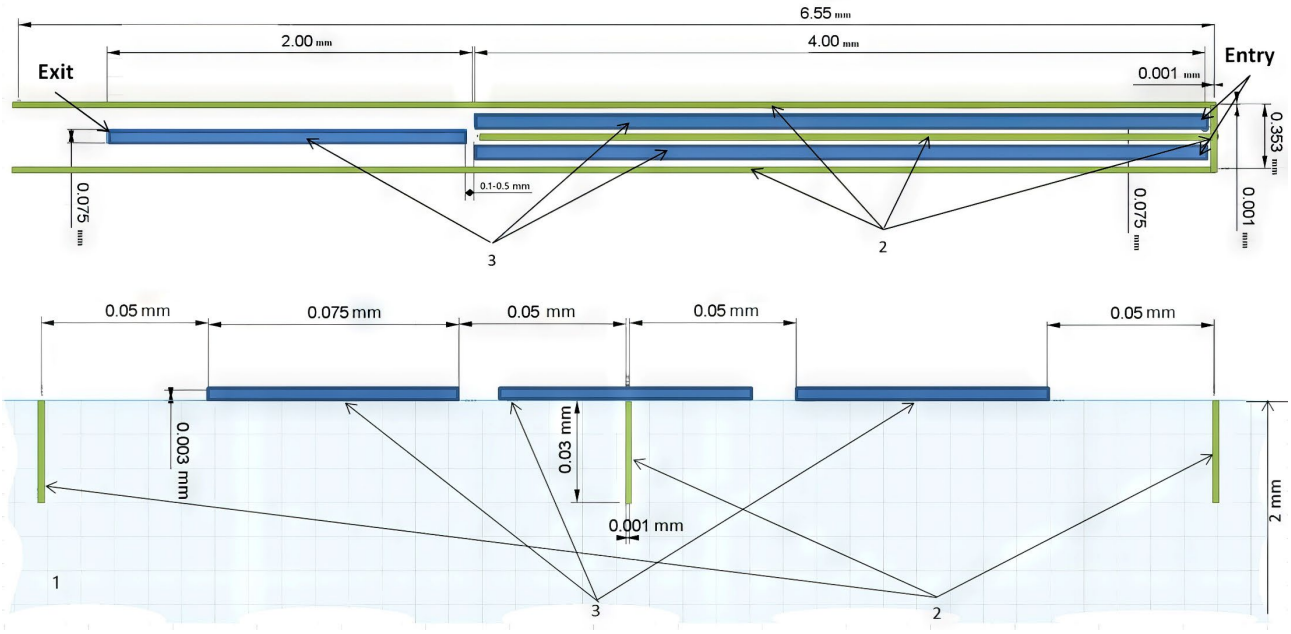

Figure 4. Structure geometry: 1- silicon wafer; 2- metal tracks for heating the structure; 3- dielectric layers (original authors' design)

The input is a logical "0" or "1". Setting a logical "1" at the output occurs because of an increase in the temperature of the memory element at the output due to the spread of the thermal field from the heated thermal memory elements with input data. Moreover, the propagation power of the thermal field must be sufficient to increase the output temperature even if a logical "1" arrives at only one element with input data on the OR logic gate. In contrast, the correct operation of a logic AND gate is based on setting a logic "1" at the output only when logic "1s" are applied to both inputs. The power of the thermal field decreases with distance from the hot body. Therefore, the logic of operation of the logic gate "OR" on the basis of thermal memory elements is realized at the expense of the minimum distance between the third element of thermal memory and elements with input data. In Figure 4, this distance is marked in the range 0.1-0.5 mm. Removal of 0.1 mm is comparable to the logic gate "OR", and the distance of 0.5 mm corresponds to the logic gate "AND".

3.2.2. Results of the Calculation of the Three-Dimensional Model

Simulation modeling made it possible to observe the distribution of thermal fields and the difference in the change in outlet temperature depending on the distance between the elements. The study of thermal field propagation was carried out at the same values of heat release power, which is set to be distributed over the volume of material of elements with input data. For the design under consideration, during the virtual experiment equal to 1 s, the power of the heat flux after 0.01 s was 7e+5 pW/μm^2, which is sufficient to transfer heat to the output of the logic gate. The required voltage to heat the input elements and set the output value was 2.5 V.

With a distance of 0.1 mm to the output element during the experiment, its temperature will reach 23.65 °C, which corresponds to an increase in temperature by two degrees from the original value. The results are shown in Figure 5. This shows the propagation of the thermal field around one memory element heated to a temperature with a maximum value on the scale is 25.767 °C. Such an increase in temperature in accordance with the material of the previously published work of the authors [3] leads to the recording of the information state of logical "1" on the memory element. The obtained result characterizes the functioning of the logic gate "OR", the value of logical "1" on any of the inputs will give a logical one on the output. And logical "1" on the output will appear in the case of two input signals equal to logical "1".

Such an operation algorithm is shown in Figure 6. Heating the two input memory elements increases the maximum temperature to 28.308 °C and, obviously, significantly increases the outlet temperature.

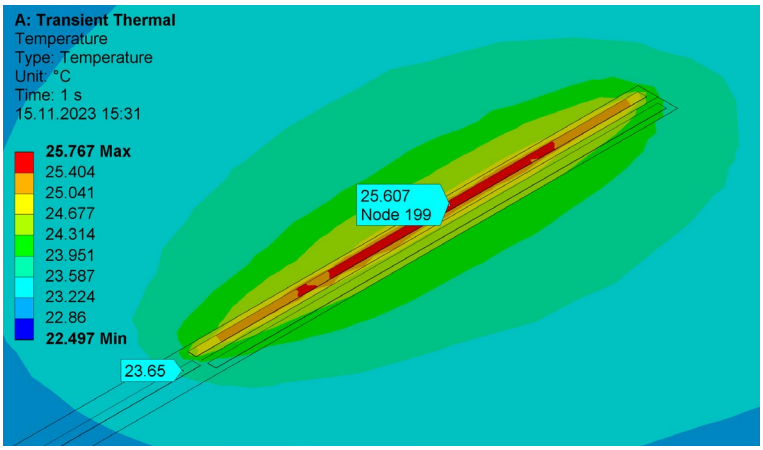

Figure 5. Propagation of the thermal field around one heated memory element to a temperature of 25.767 °C (original authors' design)

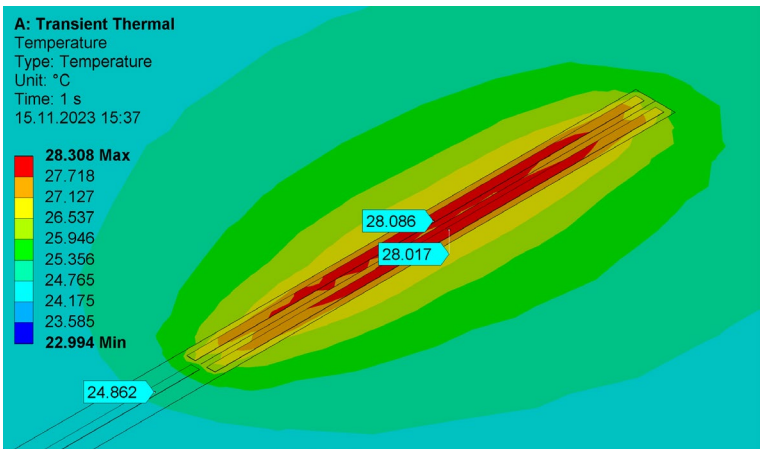

Figure 6. Heating of two memory input elements with increasing maximum temperature value up to 28.308 °C (original authors' design)

The calculations showed that at a distance of 0.5 mm from the output element, its temperature will reach the value of logic "1" only when two input memory elements are heated simultaneously. The result is presented in Figure 7. This figure shows the propagation of the thermal field around two simultaneously heated input memory elements to a temperature whose maximum value on the scale is 28.291 °C. At the same time, the output element is heated to 24.593 °C, which corresponds to an increase in the temperature of the memory material by two degrees, which also results in the information state of logical "1" being written to the memory element.

This behavior characterizes the functioning of the logic gate "AND", the output will be the value of logic "1" only in the case of arrival of logic "1" on both input memory elements. Insignificant change in the temperature at the output in the case of receipt of logic "1" only on one element with input data is shown in Figure 8.

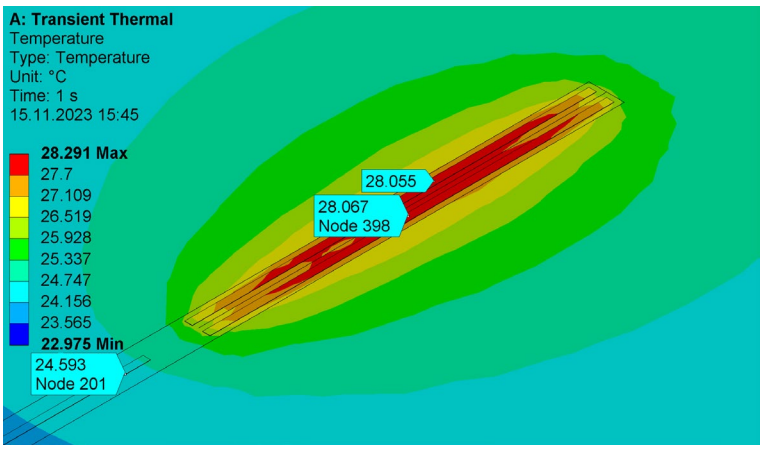

Figure 7. Thermal field propagation around two simultaneously heated memory elements with input data up to temperature 28.291 °C (original authors' design)

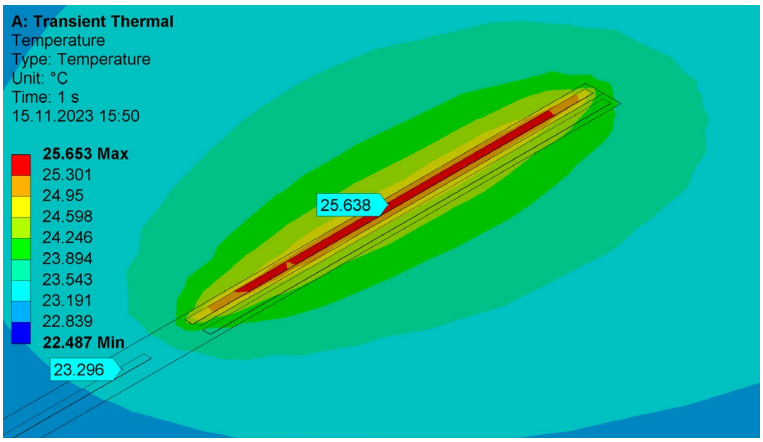

Figure 8. Increase in output temperature insufficient for switching its information state (original authors' design)

This confirms the possibility of implementing the "AND" logic gate based on thermal memory elements when the output element is removed from the input element by 0.5 mm in the design proposed by the authors.

4. RESULT (EVALUATION)

Simulation modeling of thermal field propagation from hot bodies demonstrates the influence of these thermal fields on other solid bodies. Conducted virtual experiments based on thermal memory elements have proven the possibility of using these elements to create an in-memory computing system. We designed AND and OR logic gates. Because of this research, we determined the number of thermal memory elements in the device that allowed us to perform calculations in memory. The device must consist of three specified elements with a distance between the two input elements and the output element ranging from 0.1 mm to 0.5 mm. It is also necessary to introduce a dielectric layer of thermal insulation according to the geometry given in Fig.4 to level the thermodynamic effects of the elements on each other.

A literature review of existing developments in the field of analog memory and in-memory computing systems revealed consistency in some functional parameters of the operation of thermal memory elements. Table 1 provides a comparison of the different types of analog memory with thermal.

Table 1. Example of different types of analog memory elements [17]

Form	Composition	Set voltage (V)	Reset voltage (V)	Store(s)	Number of switching	Hardiness (cycles)	Speed of work
Oxide-RRAM	$Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt$	-1	2	-	>10	10^{12}	10 ns
	$Ag/TiN/HfO_x/HfO_y/HfO_x/Pt$	-	-	-	10^{10}	10^6	60 ns
	Pt/SiO_x:Pt/Ta	~-0.6	1 – 1.2	10^7	10^3	3×10^7	<100 ps
Perovskite-RRAM	$ITO/Ag/MAPbI_3/Au$	2.4	-2.2	4.2×10^7	~ 10^7	~ 10^6	100 ps
Organic-RRAM	$ITO/Cs_2AgBiBr_6/Au$	1.53	-3.4	10^5	$>10^2$	10^3	-
	$Ag/SU\text{-}8_{Ag}/Pt$	<0.3	<0.7	2×10^3	~10^6	10^2	-
	$Ag/2DP_{BTA+PDA}/ITO$	0.90	-1	8×10^4	~10^5	2×10^2	-
	Ag/Fk-800/Pt	-	-	-	$>10^2$	$>10^6$	340 µs
	Ag/DNA/AgNP/Pt	0.3	-0.2	10^5	10^6	1000	20 ns
2D-RRAM	ITO/PVA-GO/ITO	-0.2	0.2	10^4	>10	5×10^2	-
	Ag/InSe/Ag	0.3	-0.7	3.5×10^4	4.5×10^3	3×10^2	-
	Pt/h-BN/Ag	0.3	-0.1	-	10^8	10^7	50 ns
Thermal memory	$Al/Si/SiO_2$	2.5	0	5	-	-	205 ms

The required voltage of 2.5 V for heating and setting the output value is comparable to the same parameter for memristors based on $CaTiO_3$ perovskites, a rare earth element. The thermal memory elements used are based on the Al–Si–SiO_2 structure, which is more cost-effective and suitable for integration with current ICs.

5. CONCLUSION

Our results show that the thermodynamic interaction of thermal memory elements with each other enables the construction of computational logic gates that perform memory and logic functions. Alongside the well-known memristive devices, there is the prospect of developing cross-bar arrays of thermal memory elements to create more integrated structures such as artificial neural networks. Memory computing or mem-computing is now a hot topic of research and development for many scientists. In the work of scientists from the Berlin Institute of Technology, Ney, et al. [18] combined elements that process and store data in one, built on the basis of a magnetic memory cell. In contrast to our research, the scientists were able to design a cell that can perform any of the five basic logical operations: AND, OR, NOT, NAND, and NOR. Using two input channels, the cell (depending on the direction of current in the output channel) behaves like an AND or OR element. By adding a third input channel, the researchers obtained an inverter.

Realization of NAND and NOR logic gates on the basis of selected elements of thermal memory is possible by creating an inverting logic of the work of these elements. Such logic of operation can be obtained by using the Peltier element. However, the size of the Peltier element available to us significantly exceeds the size of the thermal memory element and creates a limitation in creating an inverting logic gate.

According to the materials from Academy of Sciences in China [18], perovskite ($CaTiO_3$) is a promising material for designing the next generation of analog memory elements, due to the newly discovered ionic-electronic conductivity switched by the concentration of majority charge carriers, and the slow decay of photocurrent [19, 20]. The performance of the perovskite-based memory element remains robust under harsh conditions and withstands irradiation for 60 s with a total radiation dose 5×10^5 rad; however, there are disadvantages, such as incompatibility with CMOS processes, which limit their practical application. Our work has shown the possibility of using a thermal memory element design to create logic gates as part of worldwide research aimed at developing in-memory computing architectures. Devices based on thermal memory elements are compatible with CMOS processes.

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